UNIT-1

BASICS OF OPERATIONAL AMPLIFERS

1.1 Constant current source (Current Mirror):

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in fig 1 and collector characteristics of a CE Transistor as in fig.2

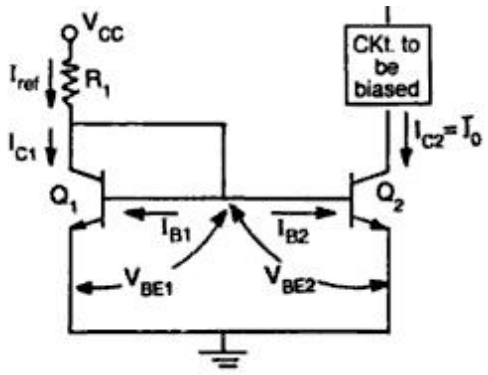


Fig. 1.1 Current mirror circuit

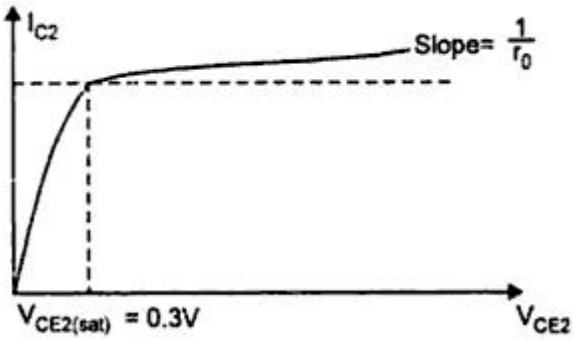


Fig 1.2 Current source output current characteristics

Transistors Q1&Q2 are matched as the circuit is fabricated using IC technology. Base and emitter of Q1& Q2 are tied together and thus have the same V_{BE}. In addition, transistor Q1 is connected as a diode by shorting its collector to base. The input current I_{ref} flows through the diode connected transistor Q1 and thus establishes a voltage across Q1. This voltage in turn appears between the base and emitter of Q2. Since Q2 is identical to Q1, the emitter current of Q2 will be equal to emitter current of Q1 which is approximately equal to I_{ref}. As long as Q2 is maintained in the active region, its collector current $I_{C2}=I_O$ will be approximately equal to I_{ref} . Since the output current Io is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

Analysis:

The collector current IC1 and IC2 for the transistor Q1 and Q2 can be approximately expressed as Where IES is reverse saturation current in emitter junction and VT is temperature equivalent of voltage.

$$I_{C1}(t)=\alpha I_{ESe}{}^{V_{BE1}/V_T} \text{ ---------- (1)}$$

$$I_{C2}(t)=\alpha I_{ESe}{}^{V_{BE2}/V_T} \text{ ---------- (2)}$$

From equation (1) & (2)

Since VBE1=VBE2 we obtain IC2=IC1=I\C=IO

Also since both the transistors are identical, IC1= IC 2

KCL at the collector of Q1 gives

$$I_{ref} = IC1+IB1+IB2$$

$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} = I_{C1} + 2\frac{I_{C1}}{\beta} \quad \text{When } I_{C1} = I_{C2} = I_C = I_o$$

Solving eq (3),

$$I_{ref} = (V_{CC} - V_{BE(ON)})/R$$

$$I_{ref} = I_{C1} + 2\frac{i_{C1}}{\beta} = I_{C1}(1 + \frac{2}{\beta})$$

$$I_C = I_{C1} = I_{C2} = \frac{I_{ref}}{1+\frac{2}{\beta}} = \frac{\beta}{\beta+2}(V_{CC} - V_{BE(ON)})/R \quad \text{---------- (5)}$$

$$I_0 = I_{ref}$$

From Eq.5 for β>>1, β/(β+ 2) is almost unity and the output current I0 is equal to the reference current, ref which for a given R_1 constant. Typically I_O varies by about 3% for $50 \leq \beta \leq 200$. The circuit however operates as a constant current source as long as Q_2 remains in the active region.

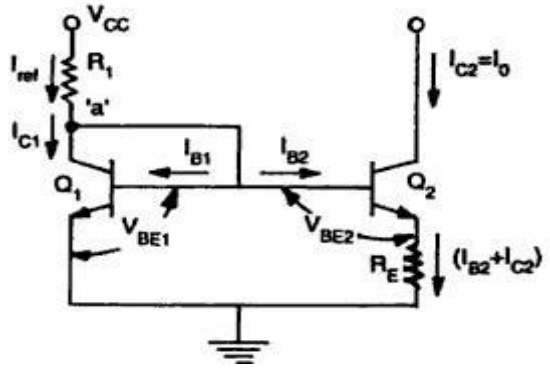


Fig.1.3 Simple current source

1.1.1 Widlar current source:

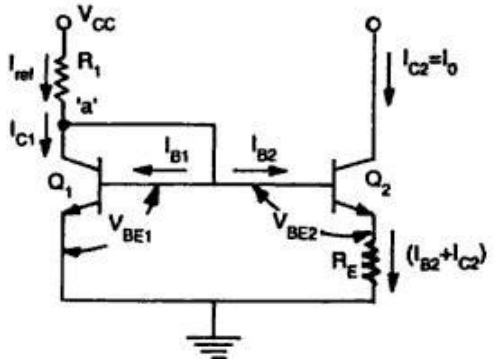


Fig.1.4 Widlar current source

Widlar current source, which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E the base-emitter voltage V_{BE2} is less than V_{BE1} and consequently current Io is smaller than I_{C1}

The ratio of collector currents IC1 and IC2 using,

$$\frac{I_{C1}}{I_{C2}} = e^{\frac{V_{BE1}-V_{BE2}}{V_T}} \quad \text{----- (1)}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\frac{I_{C1}}{I_{C2}} \quad \text{---- (2)}$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{EB2} + (I_{B2} + I_{C2})R_E \quad \text{----(3)}$$

or $$V_{BE1} - V_{BE2} = \left(\frac{1}{\beta} + 1\right) I_{C2} R_E \quad \text{--- (4)}$$

from equation (2) & (4) we obtain

$V_T \ln \frac{I_{C1}}{I_{C2}} = \left(\frac{1}{\beta} + 1\right) I_{C2} R_E$ --- (5)

A relation between IC1 and the reference current I_{ref} is obtained by writing KCL at the collector point of Q1

$$I_{ref} = I_{C1} + I_{B1} + I_{B2}$$

$$I_{ref} = I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta}$$

neglecting I_{C2}/β, $I_{ref} = I_{C1}(1 + \frac{1}{\beta})$

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1}$$

When $\beta \gg 1, I_{C1} = I_{ref}$

1.1.2 Wilson current source:

The Wilson current source shown in figure

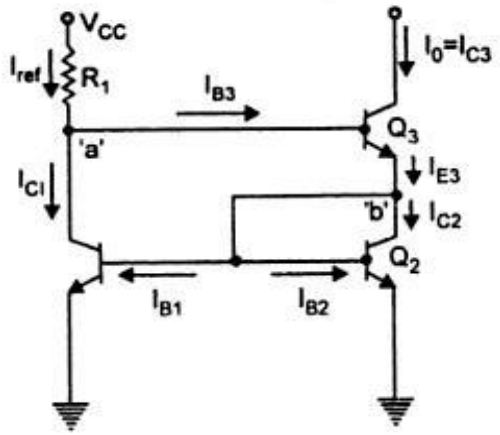


Fig.1.5 Wilson current source

It provides an output current I0 which is very nearly equal to Vref and also exhibits a very high
output resistance.

Analysis

Since $V_{BE1} = V_{BE2}$, $I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node 'b'

$I_{E3} = 2I_B + I_{C2} = (\frac{2}{\beta} + 1) I_{C2}$ ---------- (1)

I_{E2} is equal to

$I_{E3} = I_{C3} + I_{B3} = I_{C3}(1+1/\beta)$ -----(2)

From (1) and (2)

$I_{C3}(1+1/\beta) = I_{C2}(1+2/\beta)$

From equation (1) and (2) we obtain,

$I_{C3} - Io = I_{C2}(\beta+2)/(\beta+1) = I_{C1}(\beta+2)/(\beta+1)$ Since $I_{C1} = I_{C2}$.

At node 'a' $I_{ref} = I_{C1} + I_{B3} = (\beta+1/\beta+2)\, Io + Io/\beta$

$I_{ref} = \frac{\beta^2+2\beta+2}{\beta^2+2\beta} Io$ and $I_{ref} = \frac{V_{CC}-2V_{BE}}{R_1}$

$$I_o - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2}$$

I_{ref} is very small for modest β. But output resistance is greater than widlar source.

1.2 Current sources as Active loads

The current source can be used as an active load in both analog and digital IC's. The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage. The active load so achieved is basically R_0 of a PNP transistor.

1.3 Voltage Sources

A voltage source is a circuit that produces an output voltage V_0, which is independent of the load driven by the voltage source, or the output current supplied to the load. The voltage source is the circuit dual of the constant current source.

A number of IC applications require a voltage reference point with very low ac impedance and a stable dc voltage that is not affected by power supply and temperature variations. There are two methods which can be used to produce a voltage source, namely,

1. Using the impedance transforming properties of the transistor, which in turn determines the current gain of the transistor and
2. Using an amplifier with negative feedback.

1.3.1 Voltage source circuit using Impedance transformation:

The voltage source circuit using the impedance transforming property of the transistor is shown in figure. The source voltage V_S drives the base of the transistor through a series resistance R_S and the output is taken across the emitter. From the circuit, the output ac resistance looking into emitter is given by

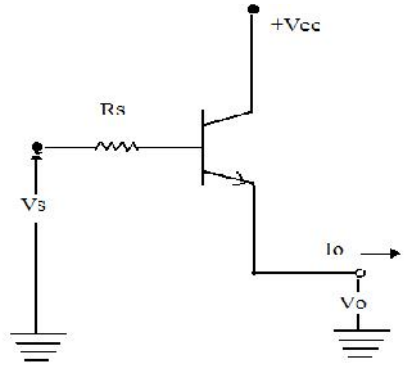


Fig.1.6 Voltage source circuit using Impedance transformation:

$$\frac{d_o}{dI_o}\Big[= R_0 = \frac{R_s}{\beta + 1} + r_{eb}$$

With β >> 100,

$$R_o = \frac{R_s}{\beta + 1}$$

It is to be noted that, equation is applicable only for small changes in the output current. The load regulation parameter indicates the changes in V_0 resulting from large changes in output current I_0 , Reduction in V_0 occurs as I_0 goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

1.3.2 Emitter– follower or Common Collector Type Voltage source:

The figure shows an emitter follower or common collector type voltage source.

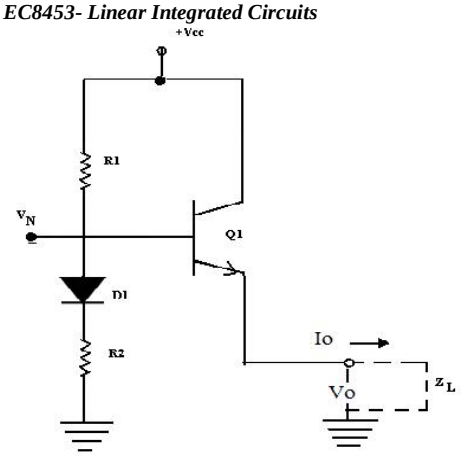


Fig.1.7 Emitter– follower or Common Collector Type Voltage source

This voltage source is suitable for the differential gain stage used in op-amps. This circuit has the advantages of

1. Producing low ac impedance and
2. Resulting in effective decoupling of adjacent gain stages.

The low output impedance of the common - collector stage simulates a low impedance voltage source with an output voltage level of Vo represented by

$$V_o = V_{cc}\frac{R_2}{R_1 + R_2}$$

The diode D_1 is used for offsetting the effect of dc value V_{BE}, across the E-B junction of the transistor, and for compensating the temperature dependence of V_{BE} drop of Q_1. The load Z_L shown in dotted line represents the circuit biased by the current through Q1.

The impedance R0 looking into the emitter of Q1 derived from the hybrid π model is given by

$$R_o = \frac{V_T}{I_1} + \frac{R_1 R_2}{\beta(R_1 + R_2)}$$

1.3.3 Voltage Source Using Temperature compensated Avalanche Diode

The voltage source using common collector stage has the limitations of its vulnerability for changes in bias voltage V_N and the output voltage V_0 with respect to changes in supply voltage Vcc. This is overcome in the voltage source circuit using the breakdown voltage of the base- emitter junction shown below. The emitter – follower stage of common – collector is eliminated in this circuit, since the impedance seen looking into the bias terminal N is very low. The current source I_1 is normally simulated by a resistor connected between Vcc and node n. Then, the output voltage level V_0 at node N is given by $V_0 = V_B + V_{BE}$ Where V_B is the breakdown voltage of diode D_B and V_{BE} is the diode drop across D_1.

The breakdown diode D_B is normally realized using the base-emitter junction of the transistor. The diode D_1 provides partial compensation for the positive temperature coefficient effect of V_B. In a monolithic IC structure, D_B and D_1 can be conveniently realized as a single transistor with two individual emitters as shown in figure.

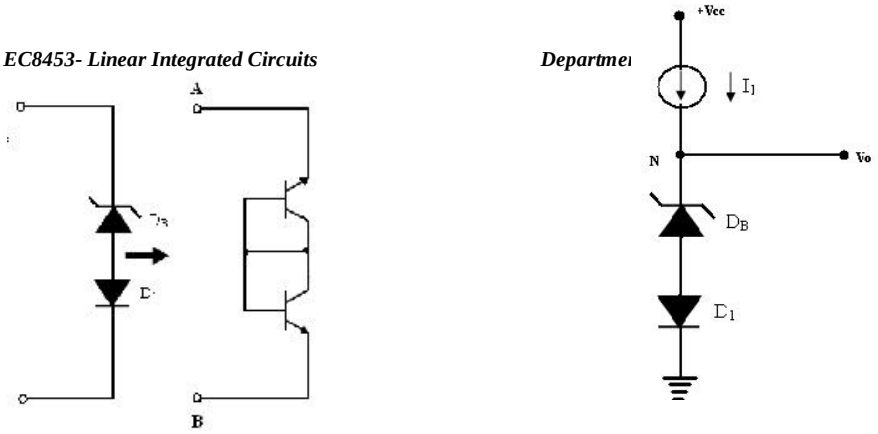


Fig.1.8 Temperature Compensated avalanche diode

1.3.4 Voltage source using breakdown voltage of the base- emitter junction

The structure consists of composite connection of two transistors which are diode-connected back-to back. Since the transistors have their base to collector terminals common, they can be designed as a single transistor with two emitters.

The output resistance R_0 looking into the output terminal in figure is given by $R_O=R_B+V_T/I_1$ where R_B and V_T /I_1 are the ac resistances of the base–emitter resistance of diode DB and D1 respectively. Typically RB is in the range of 40Ω to 100Ω, and V0 in the range of 6.5V to 9V.

1.3.5 Voltage Source using VBE as a reference:

The output stage of op-amp requires stabilized bias voltage source, which can be obtained using a forward-biased diode connected transistor. The forward voltage drop for such a connection is approximately 0.7V, and it changes slightly with current.

When a voltage level greater than 0.7V, is needed, several diodes can be connected in series, which can offer integral multiples of 0.7V. Alternatively, the figure shows a multiplier circuit, which can offer voltage levels that need not be integral multiplied of 0.7V. The drop across R_2 equals V_{BE} drop of Q_1. Considering negligible base current for Q1, current throughR2 is the same as that flowing through R1. therefore, the output voltage Vo can be expressed as

$$V_o = I_2(R_1 + R_2) = \frac{V_{BE}}{R_2}(R_1 + R_2) = V_{BE}(\frac{R_1}{R_2} + 1)$$

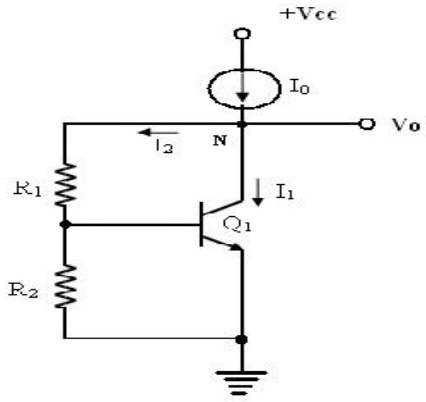


Fig.1.9 V_{BE} multiplier Circuit

Hence, the voltage V_0 can be any multiple of V_{BE} by properly selecting the resistors R_1 and R_2. Due to the shunt feedback provided by R_1, the transistor current I_1 automatically adjusts itself, towards maintaining I_2 and Vo relatively independent of the changes in supply voltage. The ac output resistance of the circuit Ro is given by,

$R_o = \frac{dV_0}{dI_o} = \frac{R_1+R_2}{1+g_mR_2} \approx \frac{R_1+R_2}{R_2g_m}$ when $g_mR_2>>1$.

$$R_0 = \frac{V_0}{V_{BE}}\frac{1}{g_m} = \frac{V_o}{V_{BE}}\frac{V_1}{I_C}\ as\ \frac{V_o}{V_{BE}} = \frac{(R_1 + R_2)}{R_2}$$

1.4 Voltage References

The circuit that is primarily designed for providing a constant voltage independent of changes in temperature is called a voltage reference. The most important characteristic of a voltage reference is the temperature coefficient of the output reference voltage TCR , and it is expressed as

$$T_{CR} = \frac{dV_R}{dT}$$

The desirable properties of a voltage reference are:

1. Reference voltage must be independent of any temperature change.
2. Reference voltage must have good power supply rejection which is as independent of the supply voltage as possible and
3. Output voltage must be as independent of the loading of output current as possible, or in other words, the circuit should have low output impedance.

The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator. The basic design strategy is producing a zero TCR at a given temperature, and thereby achieving good thermal ability.

Temperature stability of the order of 100ppm/°C is typically expected.

1.4.1 Voltage Reference circuit using temperature compensation scheme

The voltage reference circuit using basic temperature compensation scheme is shown below. This design utilizes the close thermal coupling achievable among the monolithic components and this technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

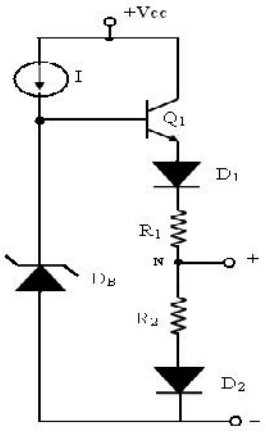


Fig.1.10 Voltage reference circuit using temperature compensation scheme

A constant current I is supplied to the avalanche diode D_B and it provides a bias voltage of V_B to the base of Q_1. The temperature dependence of the V_{BE} drop across Q_1 and those across D_1 and D_2 results in respective temperature coefficients. Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base- emitter loop of Q_1. This results in generating a voltage reference V_R with normally zero temperature coefficient.

1.4.2 Voltage Reference circuit using Avalanche Diode Reference:

A voltage reference can be implemented using the breakdown phenomenon condition of a heavily doped PN junction. The Zener breakdown is the main mechanism for junctions, which breakdown at a voltage of 5V or less. For integrated transistors, the base-emitter breakdown voltage falls in the range of 6 to 8V. Therefore, the breakdown in the junctions of the integrated transistor is primarily due to avalanche multiplication. The avalanche breakdown voltage VB of a transistor incurs a positive temperature coefficient, typically in the range of 2mV/0 C to 5mV/0 C.

Figure depicts a current reference circuit using avalanche diode reference. The base bias for transistor Q1 is provided through register R1 and it also provides the dc current needed to bias DB, D1 and D2 .The voltage at the base of Q_1 is equal to the Zener voltage V_B added with two diode drops due to D_1 and D_2. The voltage across R_2 is equal to the voltage at the base of Q_1 less the sum of the base – emitter voltages of Q_1 and Q_2.

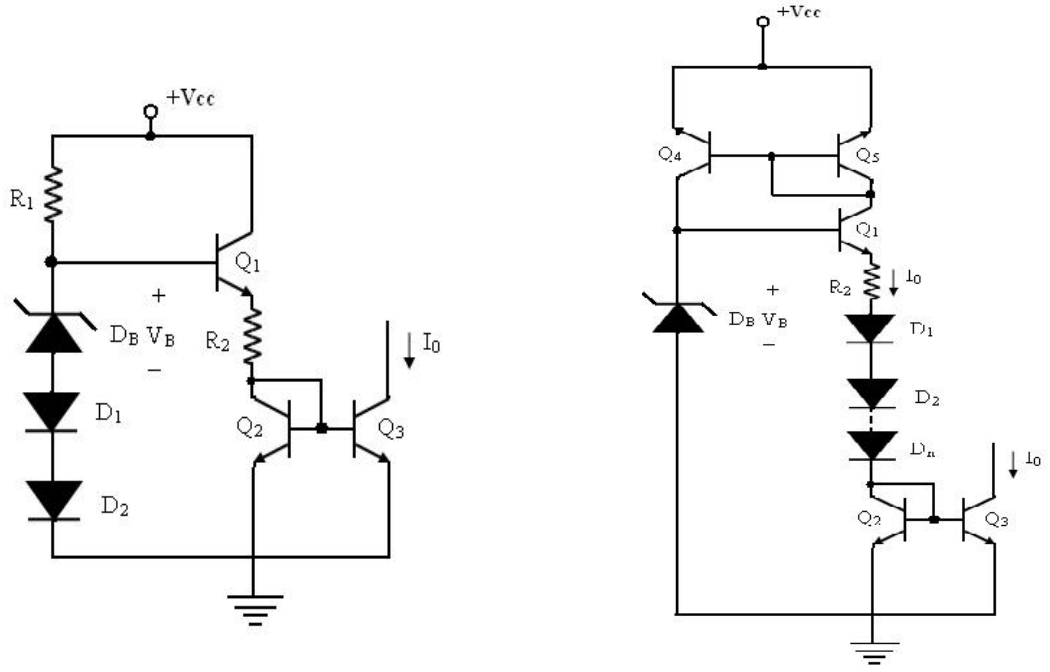


Fig. 1.11 Voltage reference using avalanche diodes and temperature compensated

Hence, the voltage across R2 is approximately equal to that across DB = VB. Since Q2 and Q3 act as a current mirror circuit, current I0 equals the current through R2.

$$I_0 = \frac{V_B}{R_2}$$

It shows that, the output current I0 has low temperature coefficient, if the temperature coefficient of R2 is low, such as that produced by a diffused resistor in IC fabrication. The zero temperature coefficients for output current can be achieved, if diodes are added in series with R2, so that they can compensate for the temperature variation of R2 and VB. The temperature compensated avalanche diode reference source circuit is shown in figure. The transistor Q4 and Q5 form an active load current mirror circuit. The base voltage of Q1 is the voltage VB across Zener DB.

Then, $V_B = (V_{BE} * n) + V_{BE}$ across $Q_1 + V_{BE}$ across Q_2 + drop across R_2. Here, n is the number of diodes.

It can be expressed as $V_B = (n+2)V_{BE} + I_0 * R_2$

Differentiating for V_B, Io,R_2 and V_{BE} partially, with respect to temperature T, we get

$$\frac{I}{I_o}\frac{\partial I_o}{\partial T} = 0 = \frac{1}{R_2 I_0}\left[\frac{\partial V_B}{\partial T} - (n+2)\frac{\partial V_{BE}}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T}\right]$$

1.5 Differential amplifier

The function of a differential amplifier is to amplify the difference between two signals. The need for differential amplifier arises in many physical measurements where response from DC to many MHz of frequency is required. This forms the basic input stage of an integrated amplifier. The basic differential amplifier has the following important properties of

Excellent stability

High versatility and

High immunity to interference signals

The differential amplifier as a building block of the op-amp has the advantages of

Lower cost

Easier fabrication as IC component and closely matched components.

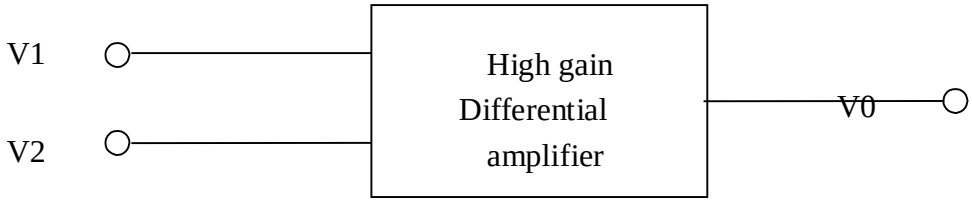


Fig. 1.12 Block diagram of Differential amplifier

The above figure shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal. The output signal of the differential amplifier is proportional to the difference between the two input signals.

$$V_0 = A_{dm}(V_1 - V_2)$$

If $V_1 = V_2$, then the output voltage is zero. A non-zero output voltage V_0 is obtained when V_1 and V_2 are not equal. The difference mode input voltage is defined as $V_m = V_1 - V_2$ and the common mode input voltage is defined as

$$V_{CM} = \frac{V_1 + V_2}{2}$$

These equation show that if $V_1 = V_2$, then the differential mode input signal is zero and common mode input signal is $V_{cm} = V_1 = V_2$.

1.5.1 Differential Amplifier with Active load:

Differential amplifier is designed with active loads to increase the differential mode voltage gain. The open circuit voltage gain of an op-amp is needed to be as large as possible. This is got by cascading the gain stages which increase the phase shift and the amplifier also becomes vulnerable to oscillations. The gain can be increased by using large values of collector resistance. For such a circuit, the voltage gain is given by

$$A_{dm} = g_m R_C$$

To increase the gain the I_C R_C product must be made very large. However, there are limitations in IC fabrication such as,

1. A large value of resistance needs a large chip area.
2. For large R_C, the quiescent drop across the resistor increase and a large power supply will be required to maintain a given operating current.
3. Large monolithic resistor introduces large parasitic capacitances which limits the

frequency response of the amplifier.

4. for linear operation of the differential pair, the devices should not be allowed to enter into saturation. This limits the max input voltage that can be applied to the bases of transistors Q_1 and Q_2 the base-collector junction must be allowed to become forward-biased by more than 0.5V. The large value of load resistance produces a large dc voltage drop (I_{EE} / 2) R_C, so that the collector voltage will be V_C=Vcc - (I_{EE}/2) R_C and it will be substantially less than the supply voltage Vcc. This will reduce the input voltage range of the differential amplifier. Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

BJT Differential Amplifier using active loads:

A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure. The active load comprises of transistors Q3 and Q4 with the transistor Q3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load R_L. When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by $I_{C4} = I_{C3} = I_{C1} = g_m V_{id}/2$ where $I_{C4} = I_{C3}$ due to current mirror action.

$I_{C2} = - g_m V_{id}/2$.

We know that the load current I_L entering the next stage is

$I_L = I_{C2} - I_{C4} = - g_m V_{id}/2 - g_m V_{id}/2 = - g_m V_{id}$

Then, the output voltage from the differential amplifier is given by $V_0 = -I_L R_L = g_m R_L V_{id}$. the ac voltage gain of the circuit is given by

$$A_V = \frac{V_o}{V_{id}} = g_m R_L$$

The amplifier can amplify the differential input signals and it provides single-ended output with a ground reference since the load RL is connected to only one output terminal. this is made possible by the use of the current mirror active load. the output resistance Ro of the circuit is that offered by the parallel combination of transistors Q2(NPN) and Q4 (PNP). It is given by Rr = ro2 || r04.

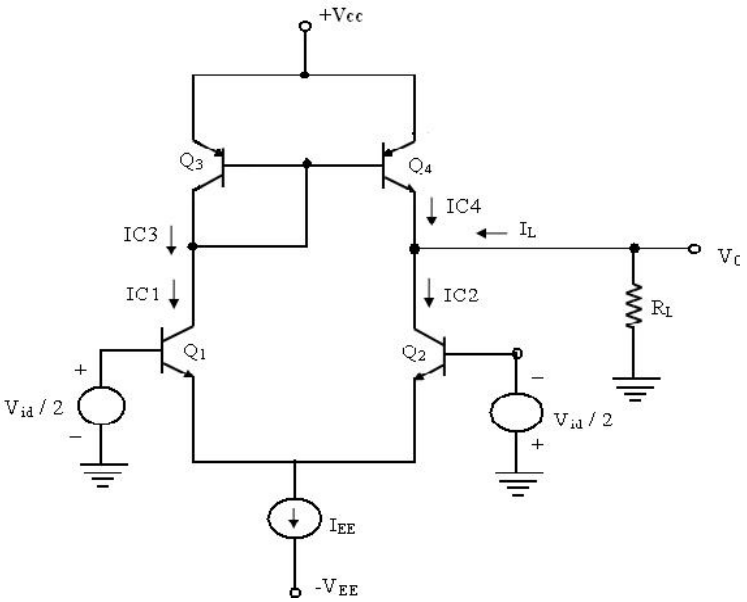


Fig. 1.13 BJT differential amplifier with current mirror active load

Analysis of BJT differential amplifier with active load:

The collector currents of all the transistors are equal.

$I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_{EE}/2$. The Collector -emitter voltages of Q1 and Q2 are given by

VCE1-VCE2 =VC-VE=V CC - VEB-(-VEB)= VCC

Eqn. shows that, the offset is higher than that of a resistive loaded differential amplifier A. This can be reduced by the use of emitter resistors for Q 3 and Q 4 , and a transistor Q5 in the current mirror load.

CMRR of the differential amplifier using active load:

The differential amplifier using active load provides high voltage gain to the differential input signal and a single – ended output that is referenced to the ground is obtained. The differential amplifier which provides conversion for a differential signal to a single ended signal is necessary in differential input signal ended output amplifiers. The op-amp is one such circuit. The changes in the common-mode signal of the bias current source. This induces a change in I_{C2} and an identical change in I_{C1}. The change in I_{C1} will then produce a change in the PNP load devices, and thereby a change in I_{C4}, which is the collector current Q4, The current I_{C4} is in such a direction as to cancel the change in I_{C2}. As a result of this, any common mode input does not cause a change in output.

The voltage gain of the differential amplifier is independent of the quiescent current I_{EE}. This makes it possible to use very small value of I_{EE} as low as 20μA, while still maintaining a large voltage gain. Small value of I_{EE} is preferred, since it results in a small value of bias current and a large value for the input resistance. A limitation in choosing a small I_{EE} is, however, the fact that, it will result in a poor frequency response of the amplifier.

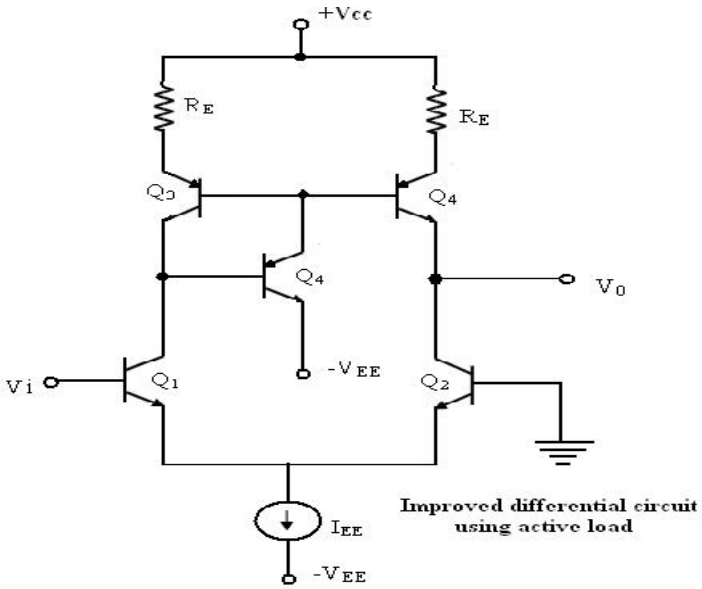


Fig.1.14. Improved differential circuit using active load

When a small value of bias current is required, the best approach is to use a JFET or MOSFET differential amplifier that is operated at comparatively higher values of I_{EE}.

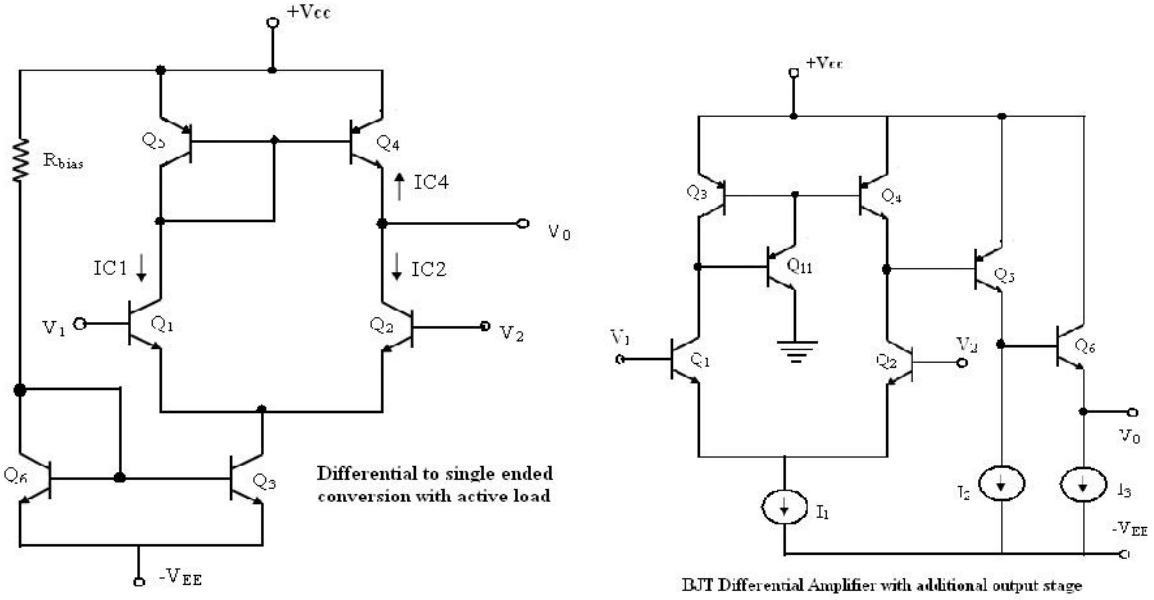


Fig.1.15. Differential to single ended conversion and output stage

Differential Mode signal analysis:

The ac analysis of the differential amplifier can be made using the circuit model as shown below. The differential input transistor pair produces equal and opposite currents whose amplitude is given by gm2 Vid/2 at the collector of Q1 and Q2. the collector current Ic1 is fed by the transistor Q3 and it is mirrored at the output of Q4. therefore, the total current Io flowing through the load resistor RL is given by Io = 2gm2 Vid / 2 = gm2 Vid.

Then the output voltage is Vo = Io RL = gm2RL Vid and the differential mode gain Adm of the differential amplifier is

$$A_{dm} = \frac{V_o}{V_{dm}} = g_{m2} R_L$$

This current mirror provides a single ended output which has a voltage equal to the maximum gain of the common emitter amplifier.

The power of the current mirror can be increased by including additional common collector stages at the o/p of the differential input stage. A bipolar differential amplifier structure with additional stages is shown in figure. The resistance at the output of the differential stage is now given by the parallel combination of transistors Q2 and Q4 and the input resistance is offered by Q5. Then, the equivalent resistance is expressed by $R_{eq} = r_{o2} \parallel r_{04} \parallel r_{i5} = r_{i5}$.

The gain of the differential stage then becomes $A_{dm} = g_m 2 R_{eq} = g_{m2} r_{i5} = \beta I_{C2}/I_{C5}$.

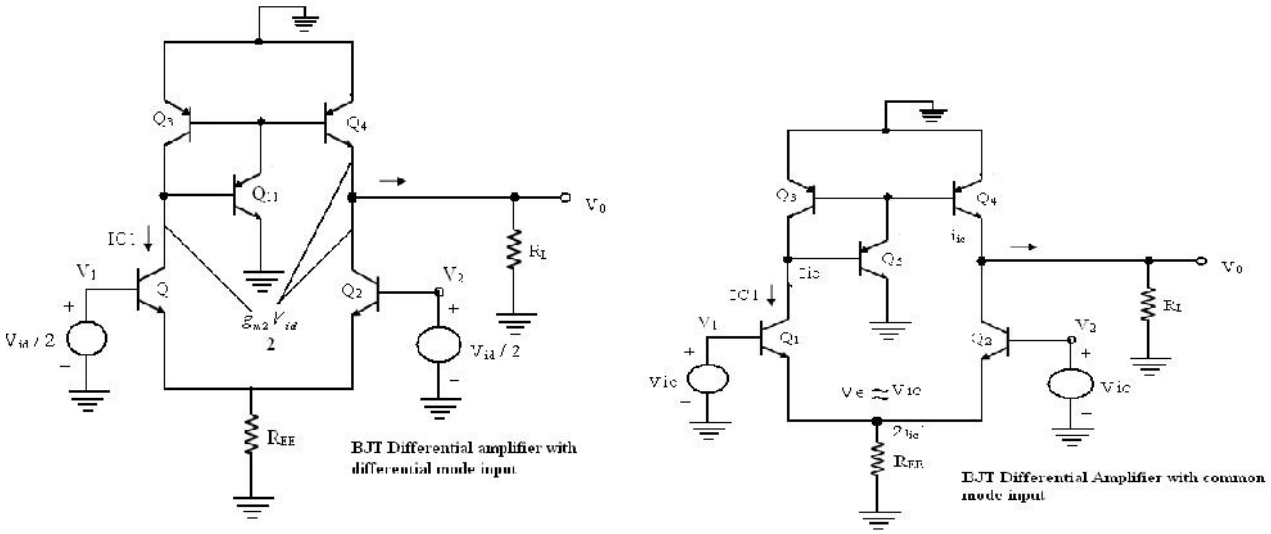
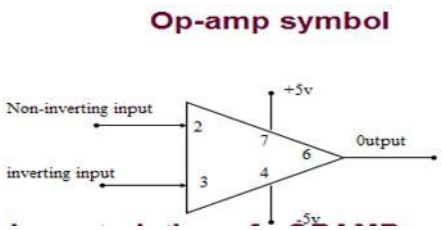


Fig. 1.16 Differential amplifier with differential mode input and common mode input

1.6 Basic information about operational amplifiers

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage. It is a versatile device that can be used to amplify ac as well as dc input signal s & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

1.7 Ideal operational Amplifiers



Ideal op-amp characteristics:

- Infinite voltage gain A.
- Infinite input resistance R_i, so that almost any signal source can drive it and there is no loading of the proceeding stage.
- Zero output resistance R_O, so that the output can drive an infinite number of other devices.
- Zero output voltage, when input voltage is zero.
- Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified without attenuation.
- Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

1.8 General Operational Amplifier stages and internal circuit diagrams of IC 741

An operational amplifier generally consists of three stages, namely

1. A differential amplifier
2. Additional amplifier stages to provide the required voltage gain and dc level shifting.
3. An emitter-follower or source follower output stage to provide current gain and low output resistance.

A low-frequency or dc gain of approximately 104 is desired for a general purpose op-amp and hence, the use of active load is preferred in the internal circuitry of op-amp. The output voltage is required to be at ground, when the differential input voltages are zero, and this necessitates the use of dual polarity supply voltage. Since the output resistance of op-amp is required to be low, a complementary push-pull emitter – follower or source follower output stage is employed. Moreover, as the input bias currents are to be very small of the order of pico amperes, an FET input stage is normally preferred.

Input stage:

The input differential amplifier stage uses p-channel JFETs M_1 and M_2. It employs a three- transistor active load formed by Q_3, Q_4, and Q_5. The bias current for the stage is provided by a two-transistor current source using PNP transistors Q_6 and Q_7. Resistor R_1 increases the o utput resistance seen looking into the collector of Q_4 as indicated by R_{04}. This is necessary to provide bias current stability against the transistor parameter variations. Resistor R_2 establishes a definite bias current through Q_5. A single ended output is taken out at the collector of Q_4.

MOSFET‘s are used in place of JFETs with additional devices in the circuit to prevent any damage for the gate oxide due to electrostatic discharges.

Gain stage:

The second stage or the gain stage uses Darlington transistor pair formed by Q_8 and Q_9 as shown in figure. The transistor Q_8 is connected as an emitter follower, providing large input resistance. Therefore, it minimizes the loading effect on the input differential amplifier stage. The transistor Q_9 provides an additional gain and Q_{10} acts as an active load for this stage. The current mirror formed by Q_7 and Q_{10} establishes the bias current for Q_9. The V_{BE} drop across Q_9 and drop across R_5 constitute the voltage drop across R_4, and this voltage sets the current through Q_8. It can be set to a small value, such that the base current of Q_8 also is very less.

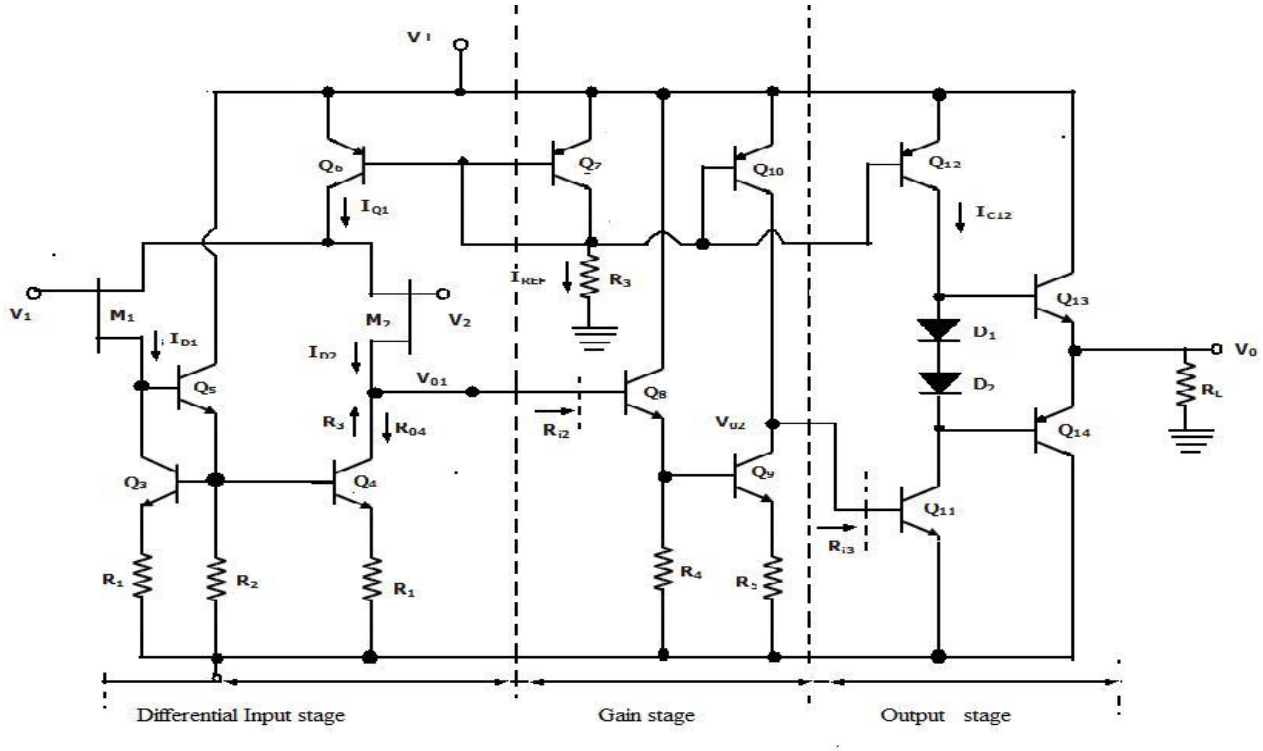


Fig. 1.17 Internal stages of Op-amp

Output stage:

The final stage of the op-amp is a class AB complementary push-pull output stage. Q_{11} is an emitter follower, providing a large input resistance for minimizing the loading effects on the gain stage. Bias current for Q_{11} is provided by the current mirror formed by Q_7 and Q_{12}, through Q_{13} and Q_{14} for minimizing the cross over distortion. Transistors can also be used in place of the two diodes. The overall voltage gain A_V of the op-amp is the product of voltage gain of each stage as given by

$A_V=|A_d|\,|A_2||A_3|$

Where A_d is the gain of the differential amplifier stage, A_2 is the gain of the second gain stage and A_3 is the gain of the output stage.

IC 741 Bipolar operational amplifier:

The IC 741 produced since 1966 by several manufactures is a widely used general purpose operational amplifier. Figure shows that equivalent circuit of the 741 op-amp, divided into various individual stages. The op-amp circuit consists of three stages.

1. The input differential amplifier
2. The gain stage
3. the output stage.

A bias circuit is used to establish the bias current for whole of the circuit in the IC. The op-amp is supplied with positive and negative supply voltages of value ± 15V and the supply voltages as low as ±5V can also be used.

Bias Circuit:

The reference bias current I_{REF} for the 741 circuit is established by the bias circuit consisting of two diodes-connected transistors Q_{11} and Q_{12} and resistor R_5. The Widlar current source formed by Q_{11}, Q_{10} and R_4 provide bias current for the differential amplifier stage at the collector of Q_{10}. Transistors Q_8 and Q_9 form another current mirror providing bias current for the differential amplifier. The reference bias current I_{REF} also provides mirrored and proportional current at the collector of the double –collector

lateral PNP transistor Q_{13}. The transistor Q_{13} and Q_{12} thus form a two-output current mirror with Q_{13A} providing bias current for output stage and Q_{13B} providing bias current for Q_{17}. The transistor Q_{18} and Q_{19} provide dc bias for the output stage. Formed by Q_{14} and Q_{20} and they establish two V_{BE} drops of potential difference between the bases of Q_{14} and Q_{18}.

Input stage:

The input differential amplifier stage consists of transistors Q_1 through Q_7 with biasing provided by Q_8 through Q_{12}. The transistor Q_1 and Q_2 form emitter – followers contributing to high differential input resistance, and whose output currents are inputs to the common base amplifier using Q_3 and Q_4 which offers a large voltage gain. The transistors Q5, Q6 and Q7 along with resistors R_1, R_2 and R_3 from the active load for input stage. The single-ended output is available at the collector of Q_6. The two null terminals in the input stage facilitate the null adjustment. The lateral PNP transistors Q3 and Q4 provide additional protection against voltage breakdown conditions. The emitter-base junction Q_3 and Q4 have higher emitter-base breakdown voltages of about 50V. Therefore, placing PNP transistors in series with NPN transistors provide protection against accidental shorting of supply to the input terminals.

Gain Stage:

The Second or the gain stage consists of transistors Q_{16} and Q_{17}, with Q_{16} acting as an emitter – follower for achieving high input resistance. The transistor Q_{17} operates in common emitter configuration with its collector voltage applied as input to the output stage. Level shifting is done for this signal at this stage.

Internal compensation through Miller compensation technique is achieved using the feedback capacitor C_1 connected between the output and input terminals of the gain stage.

Output stage:

The output stage is a class AB circuit consisting of complementary emitter follower transistor pair Q_{14} and Q_{20}. Hence, they provide an effective loss output resistance and current gain. The output of the gain stage is connected at the base of Q_{22}, which is connected as an emitter follower providing a very high input resistance, and it offers no appreciable loading effect on the gain stage. It is biased by transistor Q_{13A} which also drives Q_{18} and Q_{19}, that are used for establishing a quiescent bias current in the output transistors Q_{14} and Q_{20}.

1.9 AC Characteristics:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

1.9.1 Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth BW $=\infty$ (i.e.) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the output.

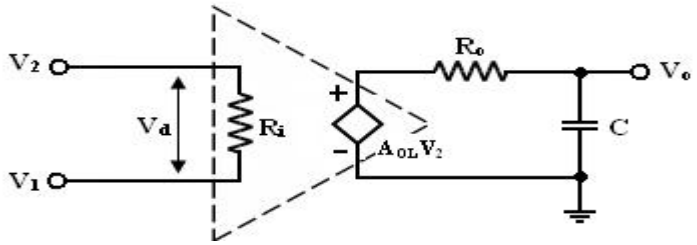


Fig 1.18 Equivalent circuit of practical circuit

There is one pole due to R_0 C and one -20dB/decade. The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase
angle of the open loop volt gain are f1 of frequency can be written as, The magnitude and phase angle characteristics:

1. For frequency $f << f_1$ the magnitude of the gain is 20 log A_{OL} in db.
2. At frequency $f = f_1$ the gain in 3 dB down from the dc value of A_{OL} in db. This frequency f_1 is called corner frequency.
3. For $f >> f_1$ the fain roll-off at the rate off -20dB/decade or -6dB/decade.

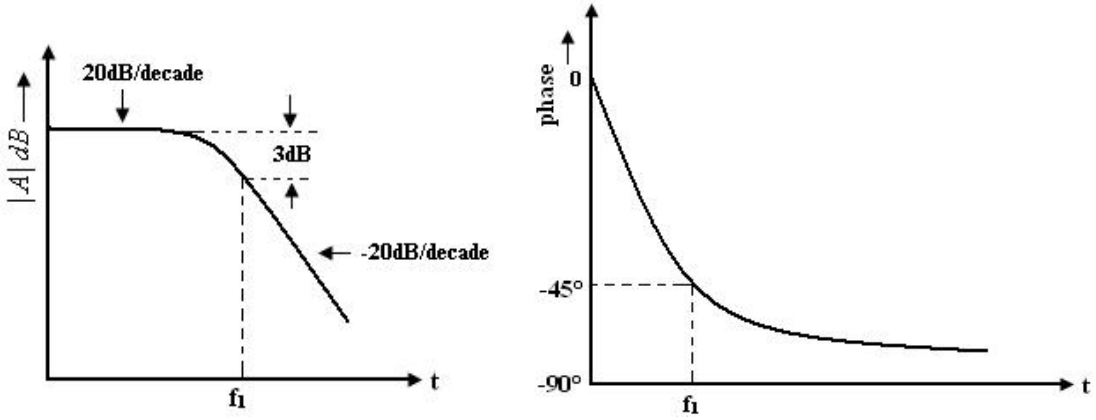


Fig 1.19 Frequency response of op amp

From the phase characteristics that the phase angle is zero at frequency f = 0. At the corner frequency f1 the phase angle is -45 (lagging and an infinite frequency the phase angle is -90 It shows that a maximum of 90 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as the decade below the corner frequency and infinite frequency is one decade above the corner frequency.

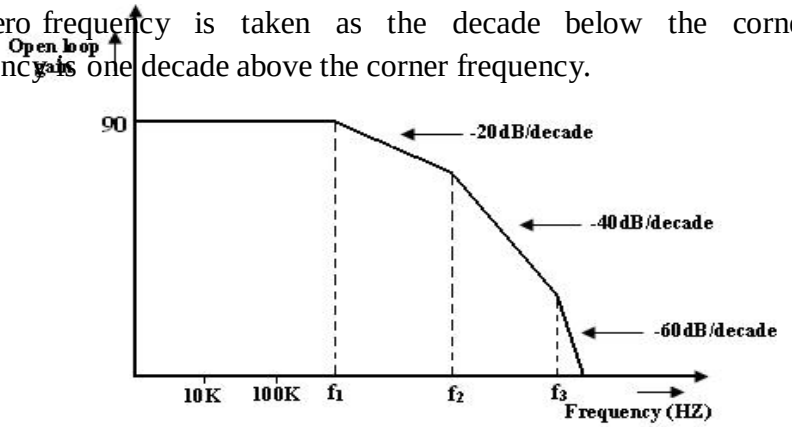


Fig. 1.20 Roll off rate of op amp gain

1.9.2 Circuit Stability:

A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system is impractical and need be made stable. The

criterion gn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability, ex: Bode plots. Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.

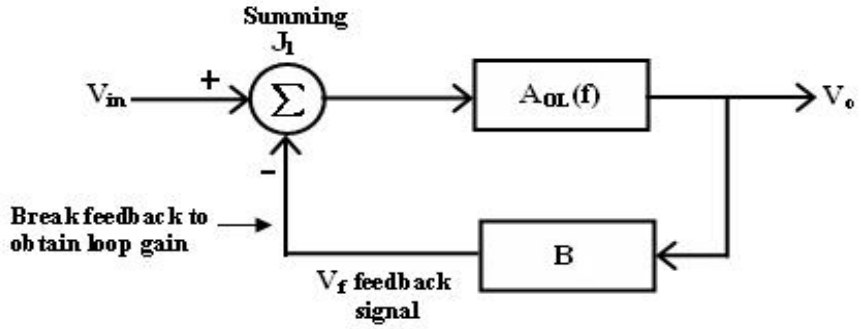


Fig. 1.21 Feedback loop system

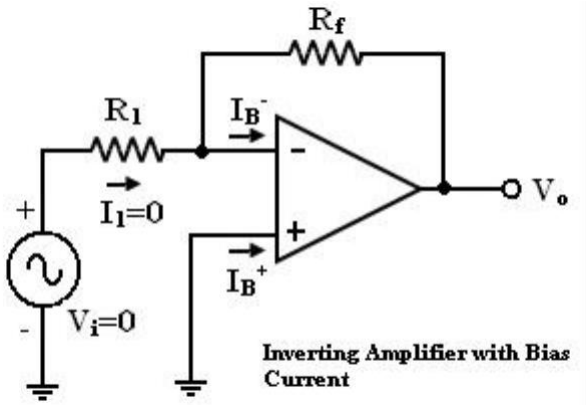
The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred as transfer frequency. From fig. we represented it by A_{OL} (f) which is given by

A_{OL} (f) = V_0 /Vin if V_f = 0 ----- (1)

where A_{OL} (f) = open loop volt gain. The closed loop gain A_f is given by

$A_F = V_0 /Vin = A_{OL} / (1+(A_{OL}) (B)$ ----(2)

B = gain of feedback circuit. B is a constant if the feedback circuit uses only resistive components.



Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

1. Method 1:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.If phase angle is >-180, the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

2. Method 2:

Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1. If phase angle is > - 180, If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

1.9.3 DC Characteristics of op-amp:

Current is taken from the source into the op-amp inputs respond differently to current and voltage due to mismatch in transistor.

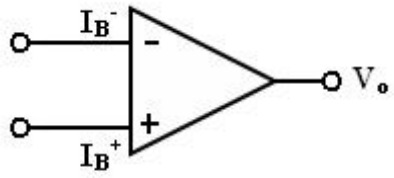
DC output voltages are,

- Input bias current

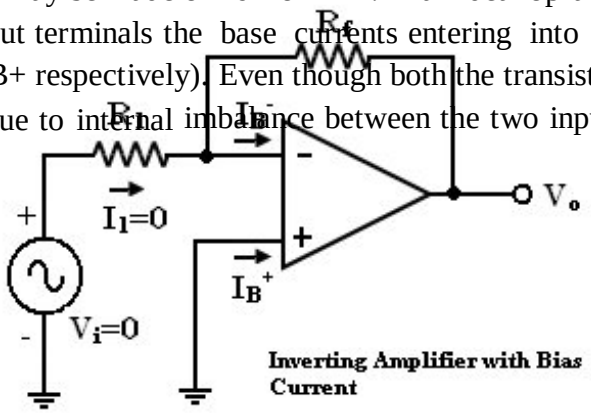
- Input offset current
- Input offset voltage
- Thermal drift

Input bias current:

The op-amp's input is differential amplifier, which may be made of BJT or FET. In an ideal op-amp, we assumed that no current is drawn from the input terminals the base currents entering into the inverting and non-inverting terminals (IB- & IB+ respectively). Even though both the transistors are identical, IB- and IB+ are not exactly equal due to internal imbalance between the two inputs. Manufacturers specify the input bias current I_B



Input Bias Current



Inverting Amplifier with Bias Current

So, $IB = (I_B^+ + I_B^-)/2$. $Vo = I_B * R_f$

If input voltage Vi = 0V. The output Voltage Vo should also be (Vo = 0) but for

IB = 500nA

We find that the output voltage is $Vo = I_B * R_f$.

Op-amp with a 1M feedback resistor Vo = 500nA X 1M = 500mV

The output is driven to 500mV with zero input, because of the bias currents. In application where the signal levels are measured in mV, this is totally unacceptable. This can be compensated by a compensation resistor Rcomp has been added between the non-inverting input terminal and ground as shown in the figure below.

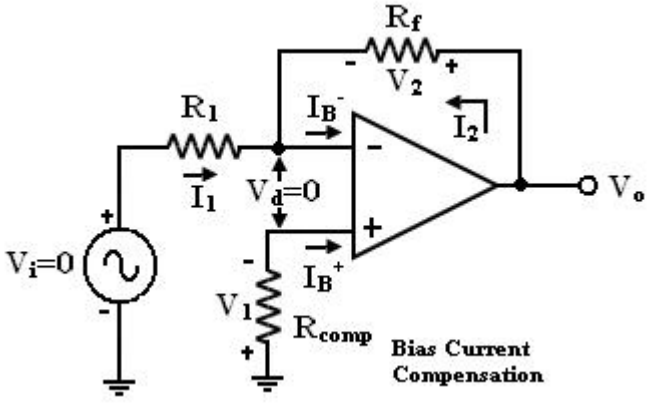


Fig. 1.22 Bias compensated circuit

Current I_B^+ flowing through the compensating resistor R_{comp}, then by KVL we get,

$-V_1+0+V_2-V_o = 0$ (or) $V_o = V_2 - V_1$ --------- (3)

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the $V_o = 0$. The value of R_{comp} is derived as $V_1 = I_B^+ R_{comp}$ (or) $I_B^+ = V_1/R_{comp}$ ---------- (4)

The node 'a' is at voltage $(-V_1)$. Because the voltage at the non-inverting input terminal is $(-V_1)$. So with $V_i = 0$ we get,

$I_1 = V_1/R_1$ ---------- (5)

$I_2 = V_2/R_f$ ---------- (6)

For compensation, V_o should equal to zero ($V_o = 0$, $V_i = 0$). i.e. from equation (3) $V_2 = V_1$.
So that, $I_2 = V_1/R_f$ ——> (7)
KCL at node 'a' gives,

$I_B^- = I_2 + I_1 = (V_1/R_f) + (V_1/R_1) = V_1(R_1+R_f)/R_1R_f$ ---------- (8)

Assume $I_B^- = I_B^+$ and using equation (4) & (8) we get

$V_1 (R_1+R_f)/R_1R_f = V_1/R_{comp}$

$R_{comp} = R_1 \parallel R_f$ ---------- (9)

i.e. to compensate for bias current, the compensating resistor, R_{comp} should be equal to the parallel combination of resistor R_1 and R_f.

Input offset current:

- Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal.
- Since the input transistor cannot be made identical. There will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current

$$|I_{os}| = I_B^+ - I_B^- \text{ ---------- (10)}$$

Offset current I_{os} for BJT op-amp is 200nA and for FET op-amp is 10pA. Even with bias current compensation, offset current will produce an output voltage when $V_i = 0$.

$V_1 = IB+ R_{comp}$ ---------- (11)

and $I_1 = V_1/R_1$ ---------- (12)

KCL at node 'a' gives $I_2 = (IB- - I_1)$

$I_2 = IB- V_1/R_1$

again $V_2 = I_2 R_f - V_1$

$V_o = I_2 R_f - I_B^+ R_{comp} = R_f I_{os}$ ------- (13)

$V_o = 1M\Omega \times 200nA$

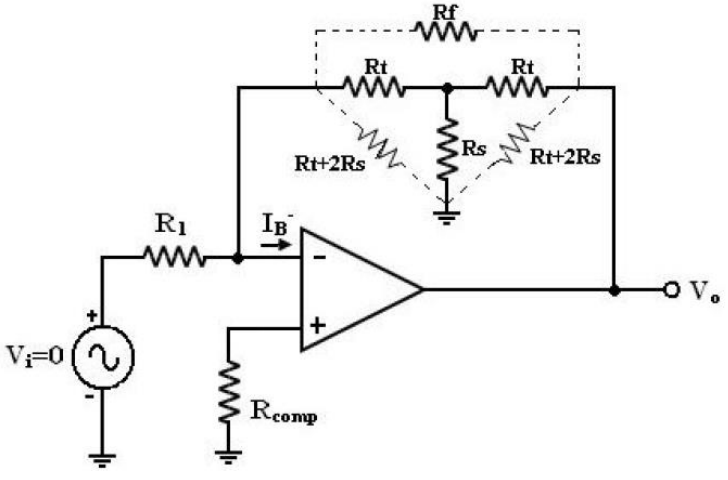
$V_o = 200mV$ with $V_i = 0$

Equation (13) the offset current can be minimized by keeping feedback resistance small.

- Unfortunately to obtain high input impedance, R_1 must be kept large.
- R_1 large, the feedback resistor R_f must also be high. So as to obtain reasonable gain.

The T-feedback network is a good solution. This will allow large feedback resistance, while keeping the resistance to ground low (in dotted line).

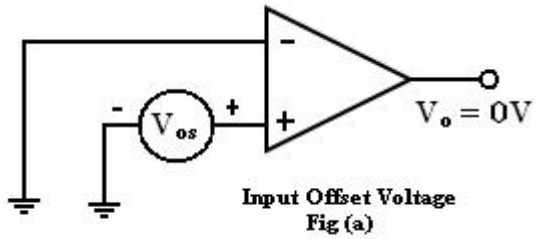
- The T-network provides a feedback signal as if the network were a single feedback resistor. By T to Π conversion.



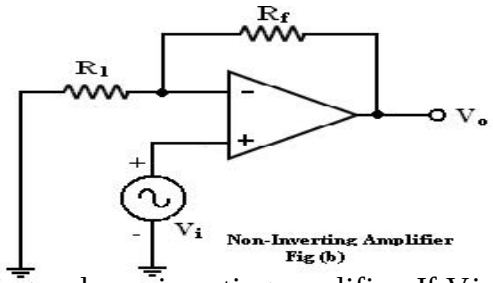
Input offset voltage:

In spite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage [$V_O \neq 0$ with $V_i = 0$]. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make output (V_O) = 0.

This voltage is called input offset voltage V_{OS}. This is the voltage required to be applied at the input for making output voltage to zero ($V_O = 0$).

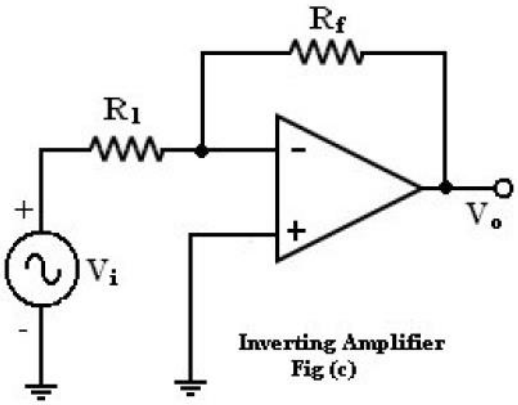


Input Offset Voltage
Fig (a)

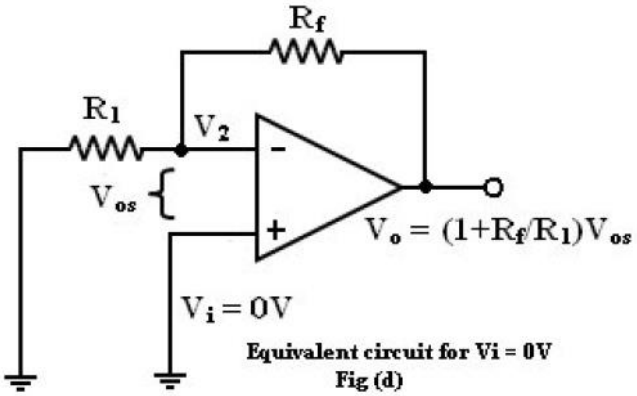


Non-Inverting Amplifier
Fig (b)

Let us determine the V_{OS} on the output of inverting and non-inverting amplifier. If $Vi = 0$ (Fig (b)
and (c)) become the same as in figure (d).



Inverting Amplifier
Fig (c)



Equivalent circuit for Vi = 0V
Fig (d)

Total output offset voltage:

The total output offset voltage VOT could be either more or less than the offset voltage produced at the output due to input bias current (IB) or input offset voltage alone(Vos). This is because IB and Vos could be either positive or negative with respect to ground. Therefore the maximum offset voltage at the output of an inverting and non-inverting amplifier (figure b, c) without any compensation technique used is given by many op amps provide offset compensation pins to nullify the offset voltage.

- A 10K potentiometer is placed across offset null pins 1&5. The wipes connected to the negative supply at pin 4.
- The position of the wipes is adjusted to nullify the offset voltage.

Thermal drift:

Bias current, offset current, and offset voltage change with temperature.

A circuit carefully nulled at 25ºC may not remain. So when the temperature rises to 35ºC. This is called drift.

Offset current drift is expressed in nA/ºC.

These indicate the change in offset for each degree Celsius change in temperature.

1.10 Slew Rate

Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs.

Reason for Slew rate:

There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ --------(1)}$$

I -> Maximum amount furnished by the op-amp to capacitor C. Op-amp should have the either a higher current or small compensating capacitors. For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is SR = dVc/Dt = Imax/C.

For a sine wave input, the effect of slew rate can be calculated as consider volt follower. The input is large amp, high frequency sine wave.

If Vs =Vm Sinwt then output V_0 = Vm sinwt .

The rate of change of output is given by dV_0/dt=Vm w coswt.

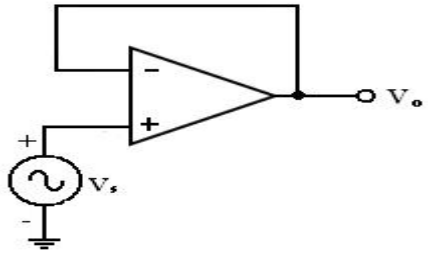


Fig. 1.22 Voltage Follower Circuit

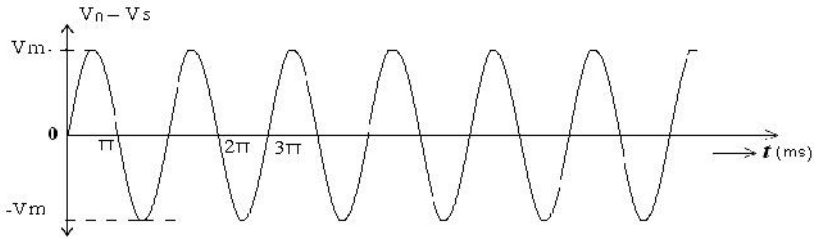


Fig. 1.23 Input and output waveforms of a voltage follower

The max rate of change of output across when

SR =dV/dt |max = Vm.

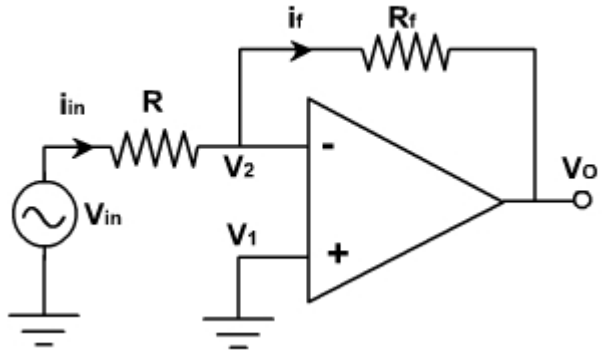
SR = 2 Vm V/s = 2 Vm V/ms. Thus the maximum frequency fmax at which undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm called the full power response. It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

UNIT II APPLICATIONS OF OPERATIONAL AMPLIFIERS

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

SCALE CHANGER:

The circuit of analog inverter is shown in fig. It is same as inverting voltage amplifier.



Assuming OPAMP to be an ideal one, the differential input voltage is zero.

i.e. $v_d = 0$

Therefore, $v_1 = v_2 = 0$

Since input impedance is very high, therefore, input current is zero. OPAMP do not sink any current.

$i_{in} = i_f$

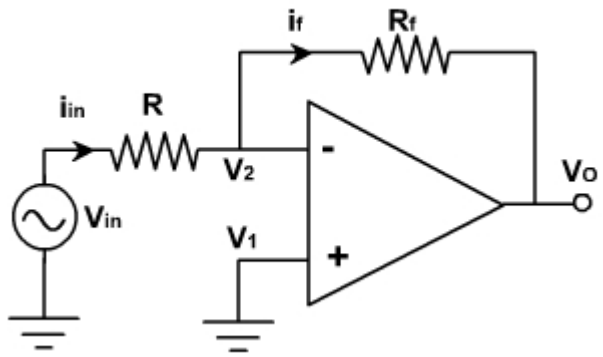
$v_{in} / R = - v_O / R_f$

$v_o = - (R_f / R) v_{in}$

If $R = R_f$ then $v_O = -v_{in}$, the circuit behaves like an inverter.

If $R_f / R = K$ (a constant) then the circuit is called inverting amplifier or scale changer voltages.

SIGN CHANGER (PHASE INVERTER)



The basic inverting amplifier configuration using an op-amp with input resistance R and feedback resistance R_f. If the resistance R and $R_f$are equal in magnitude and phase, then the closed loop voltage gain is -1,and the input signal will undergo a 180 phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign. Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

PHASE SHIFT CIRCUITS

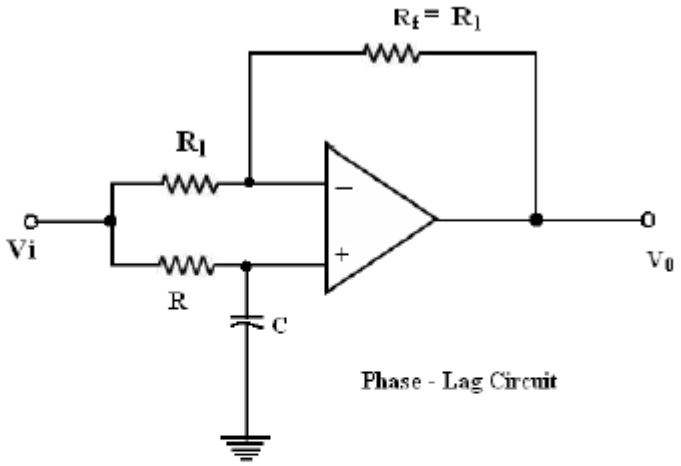
The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

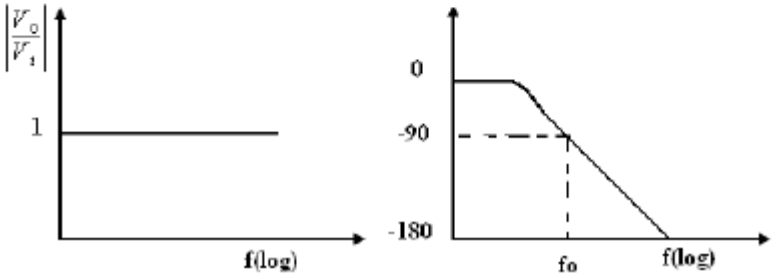
Phase-lag circuit:

Phase lag circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter. It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit

is$1 + \frac{Rf}{R1} = 1 + 1 = 2. Since\ Rf = R1$

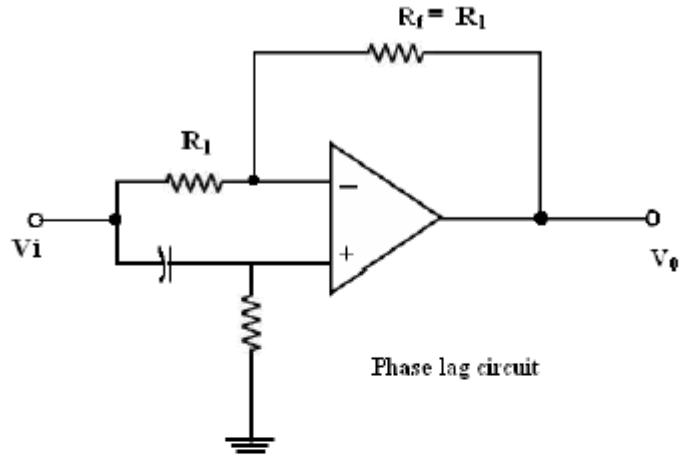


Phase - Lag Circuit

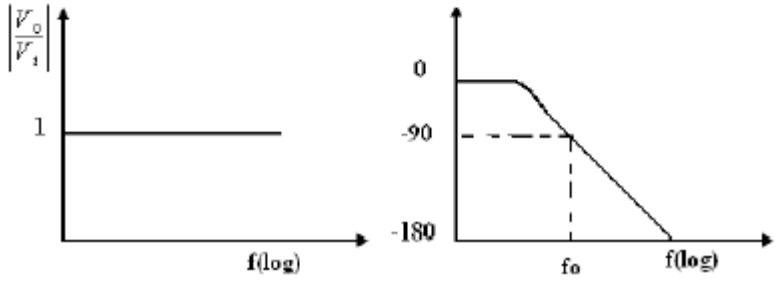


The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

Phases-lead circuit:



Bode plot for the phase-lead circuit of below fig



VOLTAGE FOLLOWER:

The lowest gain that can be obtained from a non-inverting amplifier with feedback is 1. When the non-inverting amplifier gives unity gain, it is called voltage follower because the output voltage is equal to the input voltage and in phase with the input voltage. In other words the output voltage follows the input voltage.

To obtain voltage follower, R_1 is open circuited and R_f is shorted in a negative feedback amplifier . The resultant circuit is shown in fig.

$v_{out} = Av_d = A (v_1 - v_2)$

$v_1 = v_{in}$

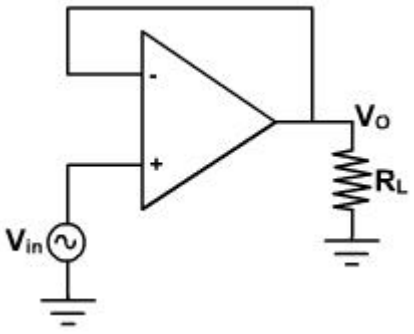
$v_2 = v_{out}$

$v_1 = v_2$ if $A >> 1$

$v_{out} = v_{in}$.

The gain of the feedback circuit (B) is 1. Therefore

$A_f = 1 / B = 1$



VOLTAGE TO CURRENT CONVERTER:

Fig, shows a voltage to current converter in which load resistor R_L is **floating** (not connected to ground).

The input voltage is applied to the non-inverting input terminal and the feedback voltage across R drives the inverting input terminal. This circuit is also called a current series negative feedback, amplifier because the feedback voltage across R depends on the output current i_L and is in series with the input difference voltage v_d.

Writing the voltage equation for the input loop.

$v_{in} = v_d + v_f$

But v_d » since A is very large,therefore,

$v_{in} = v_f$

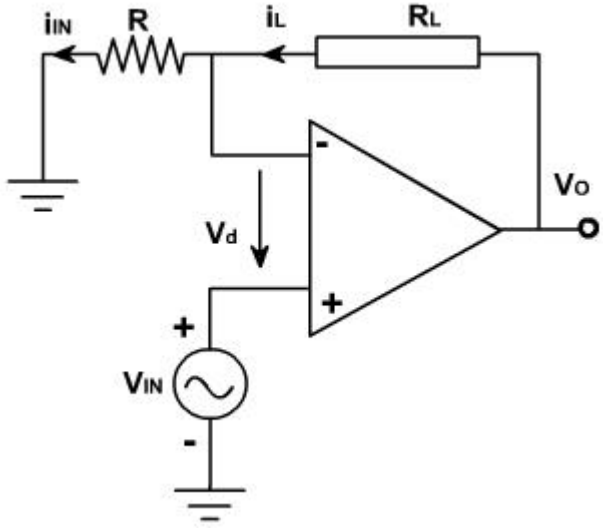
$v_{in} = R\ i_{in}$

$i_{in} = v_{in} / R.$

and since input current is zero.

$i_L = i_{in} = v_{in} ./ R$

The value of load resistance does not appear in this equation. Therefore, the output current is independent of the value of load resistance. Thus the input voltage is converted into current, the source must be capable of supplying this load current.



Grounded Load:

If the load has to be grounded, then the above circuit cannot be used. The modified circuit is shown in fig. 4

Since the collector and emitter currents are equal to a close approximation and the input impedance of OPAMP is very high,the load current also flows through the feedback resistor R. On account of this, there is still current feedback, which means that the load current is stabilized.

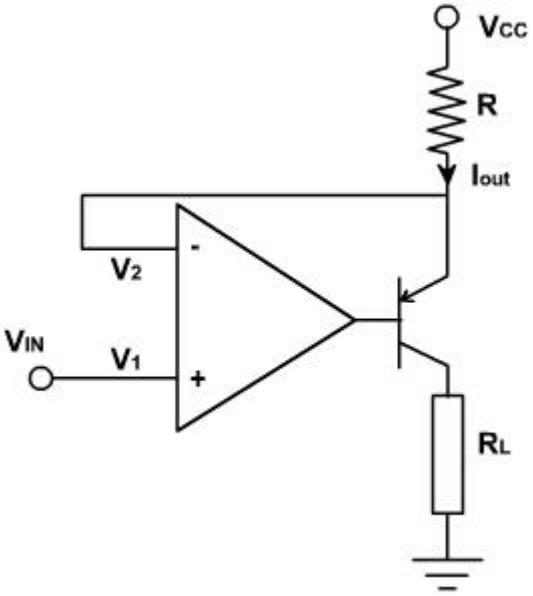
Since $v_d = 0$

$v_2 = v_1 = v_{in}$

$i_{out} = (v_{CC} - v_{in}) / R$

Thus the load current becomes nearly equal to i_{out}. There is a limit to the output current that the circuit can supply. The base current in the transistor equals i_{out} / b_{dc}. Since the op-amp has to supply this base current i_{out} / b_{dc} must be less than I_{out} (max) of the op-amp, typically 10 to 15mA.

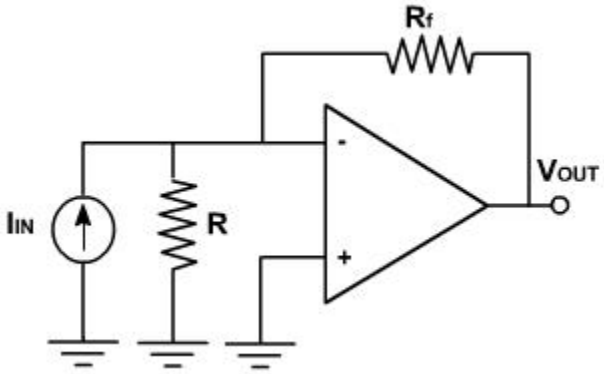
There is also a limit on the output voltage, as the load resistance increases, the load voltage increases and then the transistor goes into saturation. Since the emitter is at V_{in} w. r. t. ground, the maximum load voltage is slightly less than V_{in}.



In this circuit, because of negative feedback $V_{BE}$is automatically adjusted. For instance, if the load resistance decreases the load current tries to increase. This means that more voltage is feedback to the inverting input, which decreases V_{BE} just enough to almost completely nullify the attempted increase in load current. From the output current expression it is clear that as V_{in} increases the load current decreases.

CURRENT TO VOLTAGE CONVERTER:

The circuit shown in fig, is a current to voltage converter.



Due to virtual ground the current through R is zero and the input current flows through R_f. Therefore, $v_{out} = -R_f * i_{in}$

The lower limit on current measure with this circuit is set by the bias current of the inverting input.

INVERTING SUMMER:

The configuration is shown in fig. With three input voltages v_a, v_b &v_c. Depending upon the value of R_f and the input resistors R_a, R_b, R_c the circuit can be used as a summing amplifier, scaling amplifier, or averaging amplifier.

Again, for an ideal OPAMP, $v_1 = v_2$. The current drawn by OPAMP is zero. Thus, applying KCL at v_2 node

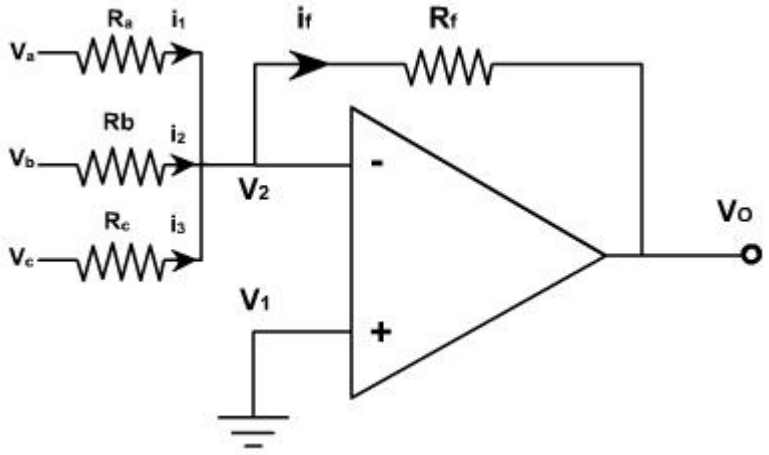
$$i_1 + i_2 + i_3 = i_f$$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_f}$$

$$V_0 = -\left(\frac{R_f}{R_a}V_a + \frac{R_f}{R_b}V_b + \frac{R_f}{R_c}v_c\right)$$

If in the circuit shown, $R_a = R_b = R_c = R$

$$V_o = -\frac{R_f}{R}(V_a + V_b + V_c)$$



This means that the output voltage is equal to the negative sum of all the inputs times the gain of the circuit R_f/ R; hence the circuit is called a summing amplifier. When R_f= R then the output voltage is equal to the negative sum of all inputs.

$v_o = -(v_a + v_b + v_c)$

If each input voltage is amplified by a different factor in other words weighted differently at the output, the circuit is called then scaling amplifier.

$$\frac{R_f}{R_a} \neq \frac{R_f}{R_b} \neq \frac{R_f}{R_c}$$

$$V_o = -\left(\frac{R_f}{R_a}V_a + \frac{R_f}{R_b}V_b + \frac{R_f}{R_c}v_c\right)$$

The circuit can be used as an averaging circuit, in which the output voltage is equal to the average of all the input voltages.

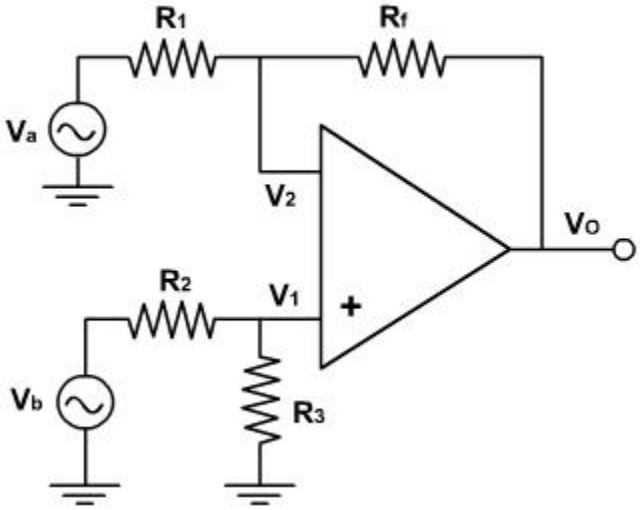
In this case, $R_a = R_b = R_c = R$ and $R_f / R = 1 / n$ where n is the number of inputs.

Here $R_f / R = 1 / 3$.

$v_o = -(v_a + v_b + v_c) / 3$

In all these applications input could be either ac or dc.

SUBTRACTOR



Since there are two inputs superposition theorem can be used to find the output voltage. When $V_b = 0$, then the circuit becomes inverting amplifier, hence the output due to V_a only is

$V_{o(a)} = -(R_f / R_1) V_a$

Similarly when, $V_a = 0$, the configuration is a inverting amplifier having a voltage divided network at the noninverting input

$$V_1 = \frac{R_3}{R_2 + R_3}V_b$$

The output due to v_b only is

$$V_{o(b)} = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}\right)V_b$$

$$= \left(\frac{R_1 + R_f}{R_1}\right)\left(\frac{R_3}{R_2 + R_3}\right)V_b$$

If $R_1 = R_2$ & $R_f = R_3$ then

$$V_{o(b)} = \frac{R_f}{R_1}V_b$$

Therefore the, total output voltage v_o is given by

$$V_o = V_{o(a)} + V_{o(b)}$$

$$V_o = \frac{R_f}{R_1}(-V_a + V_b)$$

If $R_f=R_1$ Then $V_o=V_b-V_a$

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is intended for precise, low-level signal amplification where high input resistance, low noise and accurate closed-loop gain is required. Also, low power consumption, high slew rate and high common-mode rejection ratio are desirable for good performance.

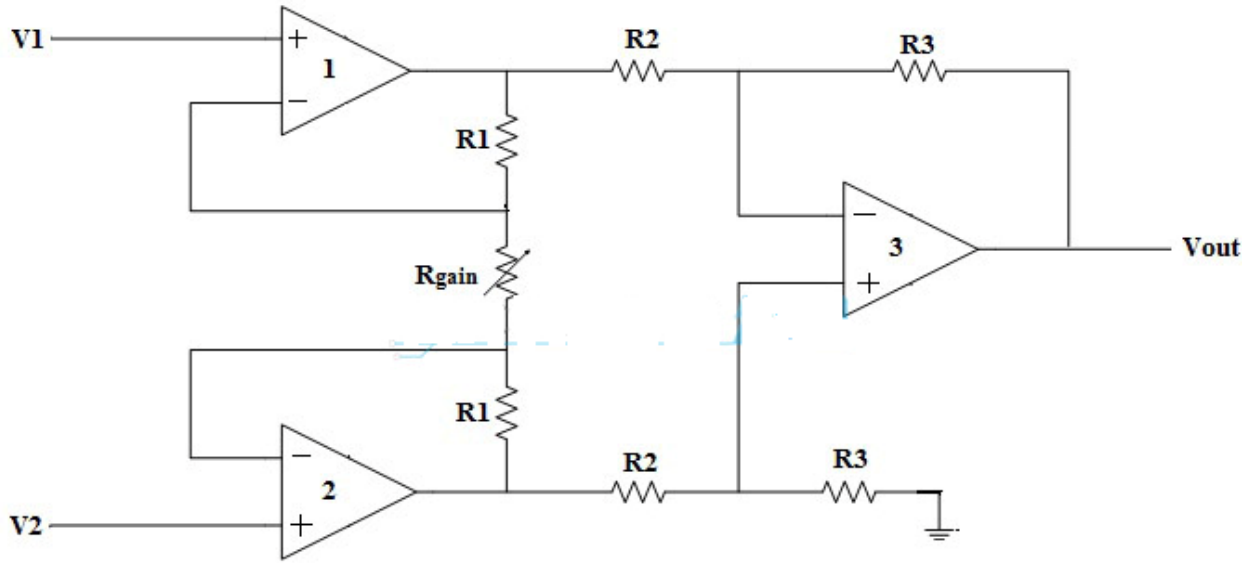
Requirements of a Good Instrumentation Amplifier

Finite, Accurate and Stable Gain
Easier Gain Adjustment
High Input Impedance
Low Output Impedance
High CMRR
High Slew Rate

Three Op-Amp Instrumentation Amplifier:

The most commonly used Instrumentation amplifiers consist of three op-amps. In this circuit, a non-inverting amplifier is connected to each input of the differential amplifier.

This instrumentation amplifier provides high input impedance for exact measurement of input data from transducers . The circuit diagram of an instrumentation amplifier is as shown in the figure below.



A Typical Three Op-amp Instrumentation Amplifier

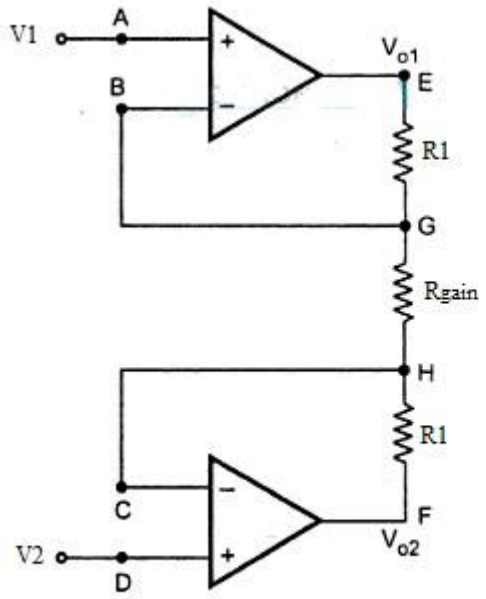
The op-amps 1 & 2 are non-inverting amplifiers and together form an input stage of the instrumentation amplifier. The op-amp 3 is a difference amplifier that forms the output stage of the instrumentation amplifier.

Working of Instrumentation Amplifier:

The output stage of the instrumentation amplifier is a difference amplifier, whose output V_{out} is the amplified difference of the input signals applied to its input terminals. If the outputs of op-amp 1 and op-amp 2 are V_{o1} and V_{o2} respectively, then the output of the difference amplifier is given by,

$$\mathbf{V_{out} = (R_3/R_2)(V_{o1}-V_{o2})}$$

The expressions for Vo1 and Vo2 can be found in terms of the input voltages and resistances. Consider the input stage of the instrumentation amplifier as shown in the figure below.



Input Stage of Instrumentation Amplifier

The potential at node A is the input voltage V_1. Hence the potential at node B is also V_1, from the virtual short concept. Thus, the potential at node G is also V_1.

The potential at node D is the input voltage V_2. Hence the potential at node C is also V_2, from the virtual short. Thus, the potential at node H is also V_2.

Ideally the current to the input stage op-amps is zero. Therefore the current *I* through the resistors R_1, R_{gain} and R_1 remains the same.

Applying Ohm's law between the nodes E and F,

$I = (V_{o1}-V_{o2})/(R_1+R_{gain}+R_1)$ ——————— 1

$I = (V_{o1}-V_{o2})/(2R_1+R_{gain})$

Since no current is flowing to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

$I = (V_G-V_H)/R_{gain} = (V_1-V_2)/R_{gain}$ ——————————- 2

Equating equations 1 and 2,

$(V_{o1}-V_{o2})/(2R_1+R_{gain}) = (V1-V_2)/R_{gain}$

$(V_{o1}-V_{o2}) = (2R_1+R_{gain})(V_1-V_2)/R_{gain}$ ——————— 3

The output of the difference amplifier is given as,

$V_{out} = (R_3/R_2)\ (V_{o1}-V_{o2})$

Therefore, $(V_{o1} – V_{o2}) = (R_2/R_3)V_{out}$

Substituting $(V_{o1} – V_{o2})$ value in the equation 3, we get

$(R_2/R_3)V_{out} = (2R_1+R_{gain})(V1-V_2)/R_{gain}$

i.e. $V_{out} = (R_3/R2)\{(2R_1+R_{gain})/R_{gain}\}(V1-V_2)$

The above equation gives the output voltage of an instrumentation amplifier. The overall gain of the amplifier is given by the term $(R_3/R2)\{(2R_1+R_{gain})/R_{gain}\}$.

Note: The overall voltage gain of an instrumentation amplifier can be controlled by adjusting the value of resistor R_{gain}. The common mode signal attenuation for the instrumentation amplifier is provided by the difference amplifier.

Advantages of Three Op-amp Instrumentation Amplifier:

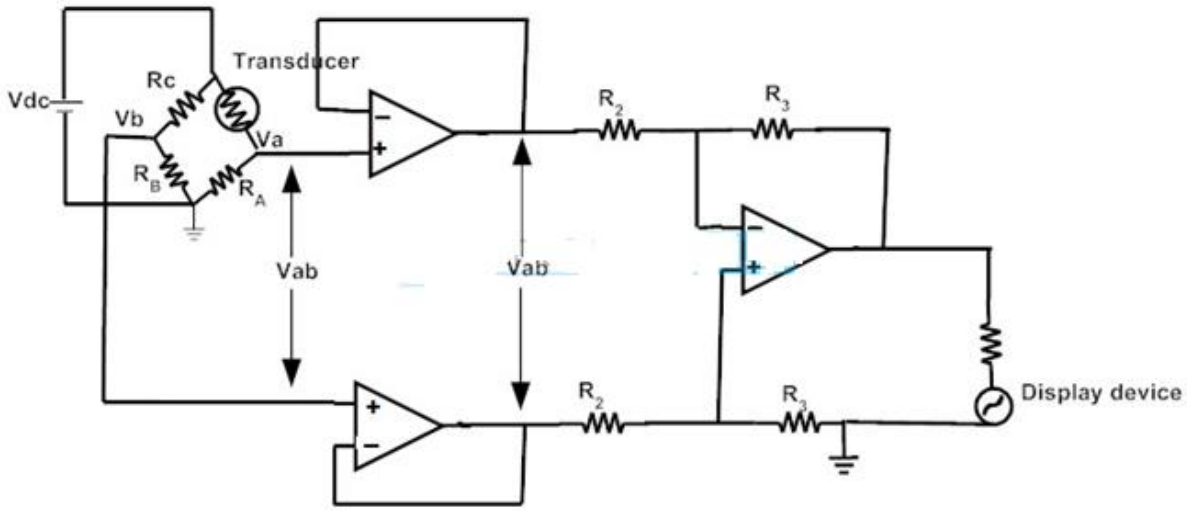
- The gain of a three op-amp instrumentation amplifier circuit can be easily varied and controlled by adjusting the value of R_{gain} without changing the circuit structure.
- The gain of the amplifier depends only on the external resistors used. Hence, it is easy to set the gain accurately by choosing the resistor values carefully.
- The input impedance of the instrumentation amplifier is dependent on the non-inverting amplifier circuits in the input stage. The input impedance of a non-inverting amplifier is very high.
- The output impedance of the instrumentation amplifier is the output impedance of the difference amplifier, which is very low.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

Transducer Bridge Instrumentation Amplifier:

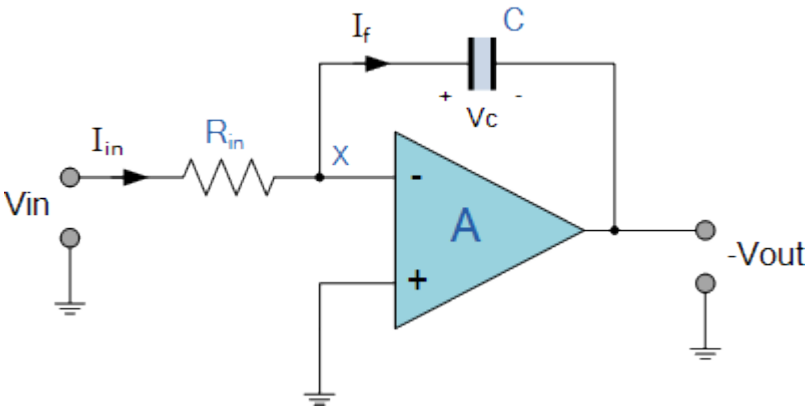
The resistive transducer bridge is a network of resistors whose resistance varies due to changes in some physical condition. For example, Thermistors change their resistance with temperature and Light Dependent Resistors change their resistance to change in light intensity.

By making such a bridge as a part of the circuit, it is possible to produce an electrical signal proportional to the change in the physical quantity being measured.

Such an electrical signal can be amplified and used to monitor and control the physical process. An instrumentation amplifier can be constructed with a transducer bridge connected to one of its input terminals, as shown in the figure below.



INTEGRATOR CIRCUIT



As its name implies, the Op-amp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration**,** that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces *an* output voltage which is proportional to the integral of the input voltage.

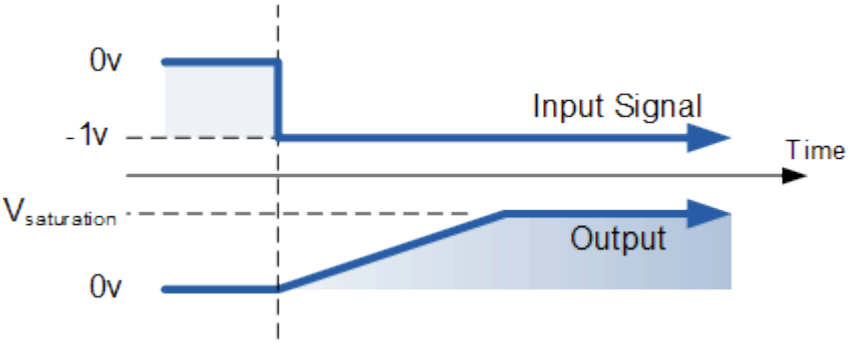
In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of X_C/R_{IN} is also very small giving an overall voltage gain of less than one, (voltage follower circuit).

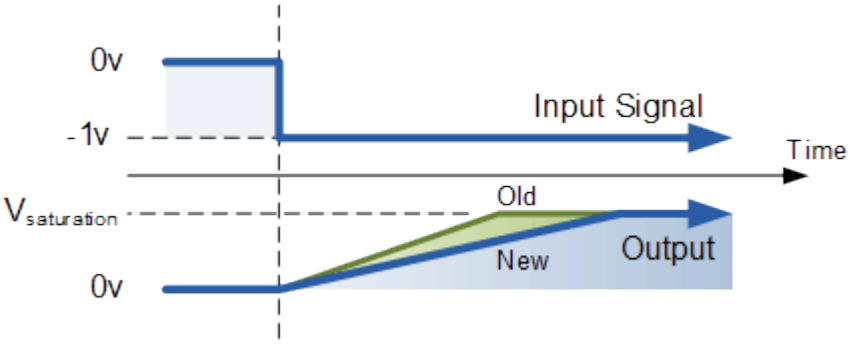
As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, (τ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.

Since the capacitor is connected between the op-amp's inverting input (which is at earth potential) and the op-amp's output (which is negative), the potential voltage, Vc developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor (X_C/R_{IN}) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

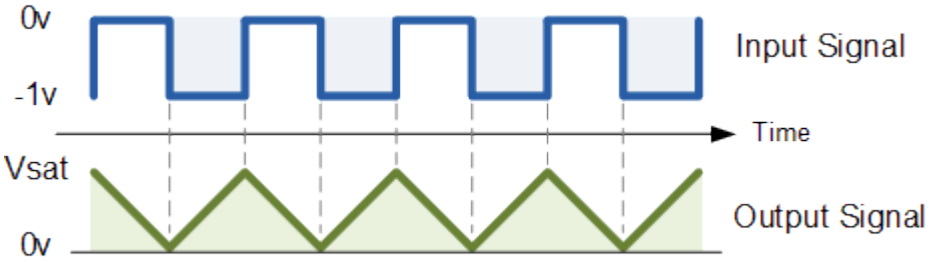


The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed for example.



If we apply a constantly changing input signal such as a square wave to the input of an **Integrator Amplifier** then the capacitor will charge and discharge in response to changes in the input signal. This results in the output signal being that of a sawtooth waveform whose output is affected by the RC time constant of the resistor/capacitor combination because at higher frequencies, the capacitor has less time to fully charge. This type of circuit is also known as a **Ramp Generator** and the transfer function is given below.

Op-amp Integrator Ramp Generator



We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, Rin is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

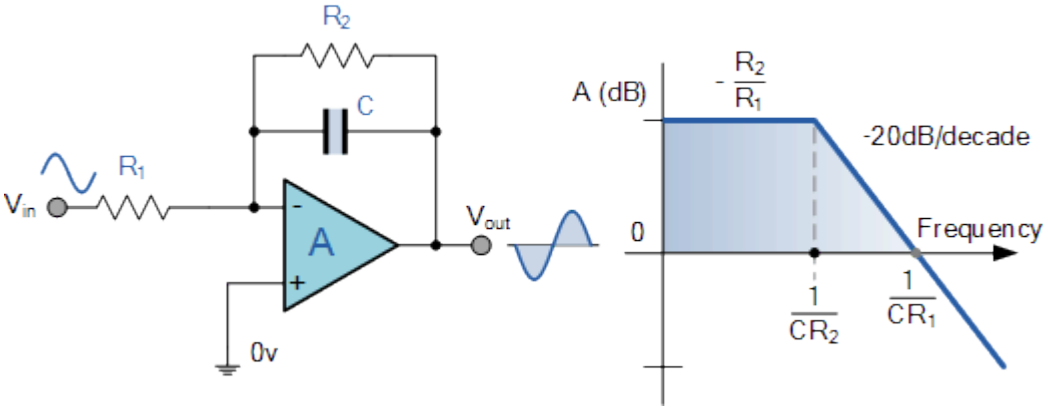
$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

Where: $\omega = 2\pi f$ and the output voltage Vout is a constant 1/RC times the integral of the input voltage Vin with respect to time. The minus sign (–) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

The AC Op-amp Integrator with DC Gain Control



Unlike the DC integrator amplifier above whose output voltage at any instant will be the integral of a waveform so that when the input is a square wave, the output waveform will be triangular. For an AC integrator, a sinusoidal input waveform will produce another sine wave as its output which will be 90° out-of-phase with the input producing a cosine wave.

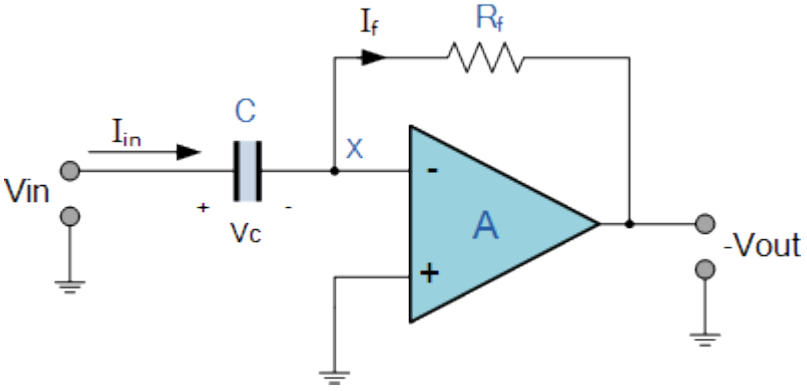
Further more, when the input is triangular, the output waveform is also sinusoidal. This then forms the basis of a Active Low Pass Filter as seen before in the filters section tutorials with a corner frequency given as.

$$\text{D.C. Voltage Gain, } (Av_o) = -\frac{R_2}{R_1}$$

$$\text{A.C. Voltage Gain, } (Av) = -\frac{R_2}{R_1} \times \frac{1}{(1+2\pi fCR_2)}$$

$$\text{Corner Frequency, } (f_o) = \frac{1}{2\pi CR_2}$$

DIFFERENTIATOR CIRCUIT



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R*f*/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R*f*.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

butdQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

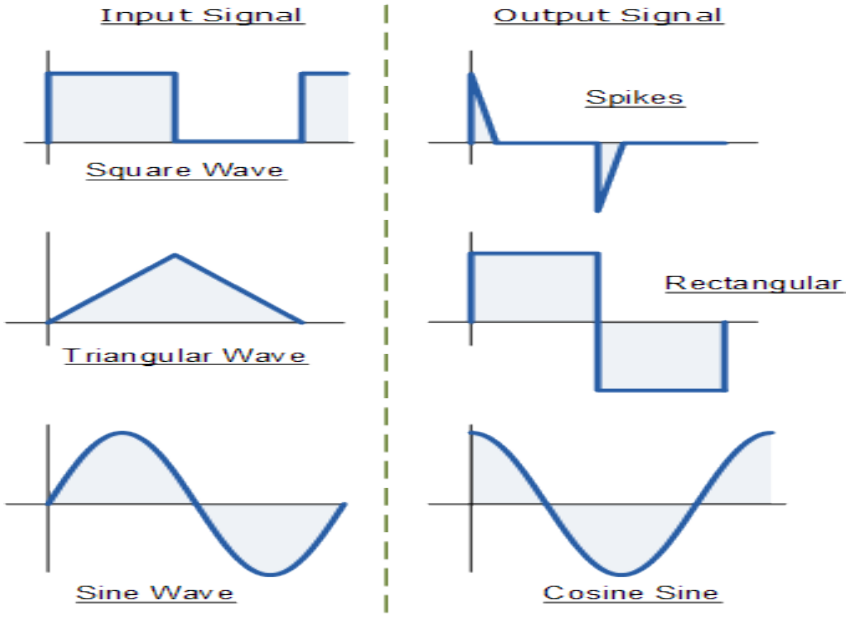
$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant –R*f**C times the derivative of the input voltage Vin with respect to time. The minus sign (–) indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

One final point to mention, the **Op-amp Differentiator** circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required.

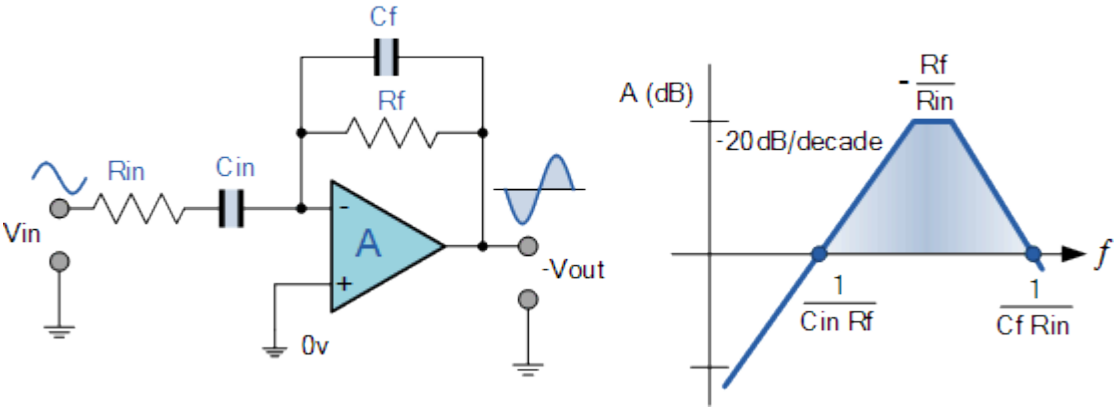
Op-amp Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.



Practical Differentiator Amplifier

The basic single resistor and single capacitor op-amp differentiator circuit is not widely used to reform the mathematical function of Differentiation because of the two inherent faults mentioned above, “Instability” and “Noise”. So in order to reduce the overall closed-loop gain of the circuit at high frequencies, an extra resistor, Rin is added to the input as shown below



Adding the input resistor R_{IN} limits the differentiators increase in gain at a ratio of Rf/R_{IN}The circuit now acts like a differentiator amplifier at low frequencies and an amplifier with resistive feedback at high frequencies giving much better noise rejection.

Additional attenuation of higher frequencies is accomplished by connecting a capacitor C*f* in parallel with the differentiator feedback resistor, R*f*. This then forms the basis of a Active High Pass Filter as we have seen before in the filters section.

LOGARITHMIC AMPLIFIER

An operational amplifier can be configured to function as a Logarithmic amplifier, or simply Log amplifier. Log amplifier is a non-linear circuit configuration, where the output is *K* times the logarithmic value of the input voltage applied. Log amplifiers find the applications in computations such as multiplication and division of signals, computation of powers and roots, signal compression and decompression, as well as in process control in industrial applications. A log amplifier can be constructed using a bipolar junction transistor in the feedback to the op-amp, since the collector current of a BJT is logarithmically related to its base-emitter voltage.

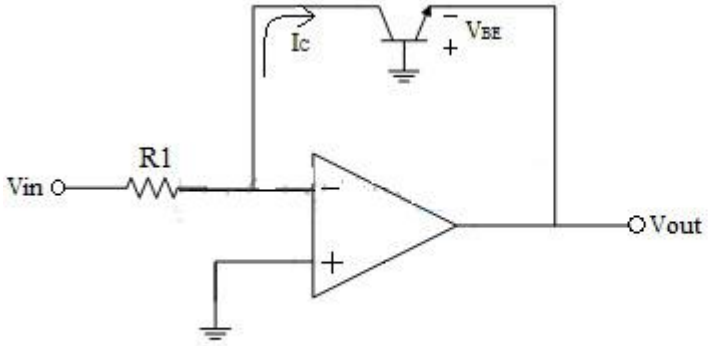


Fig: Op-amp Logarithmic Amplifier

The circuit of a fundamental log amplifier using op-amp is shown in the figure above. The necessary condition of the log amplifier to work is that the input voltage always must be positive. It can be seen that $V_{out} = – V_{be}$.

Since the collector terminal of the transistor is held at virtual ground and the base terminal is also grounded, the voltage-current relationship becomes that of a diode and is given by,

$I_E = I_S.[e^{q(Vbe)/kT} – 1]$

Where,

I_S = the saturation current,

k = Boltzmann's constant

T = absolute temperature (in K)

Since $I_E = I_C$ for grounded base transistor,

$I_C = I_S. [e^{q(Vbe)/kT} – 1]$

$(I_C/I_S) = [e^{q(Vbe)/kT} – 1]$

$(I_C/I_S) + 1 = [e^{q(Vbe)/kT}]$

$(I_C+I_S)/I_S = e^{q(Vbe)/kT}$

$e^{q(Vbe)/kT} = (I_C/I_S)$ since $I_C >> I_S$

Taking natural log on both sides of the above equation, we get

$V_{be} = (kT/q) \ln[I_C/I_S]$

The collector current $I_C = V_{in}/R_1$ and $V_{out} = -V_{be}$

Therefore,

$V_{out} = -(kT/q) \ln[V_{in}/R_1.I_S]$

The output of the circuit is, thus, proportional to the log of the input voltage. However, the output is dependent on the saturation current which varies from transistor to transistor and also with temperature. Compensation circuits can be added to stabilize the output against these variations.

ANTI-LOGARITHMIC AMPLIFIER

Anti-logarithmic or exponential amplifier (or simply antilog amplifier) is an op-amp circuit configuration, whose output is proportional to the exponential value or anti-log value of the input. Antilog amplifier does the exact opposite of a log amplifier. Antilog amplifiers along with log amplifiers are used to perform analogue computations on the input signals. The circuit of an antilog amplifier using op-amp is shown in the figure below.

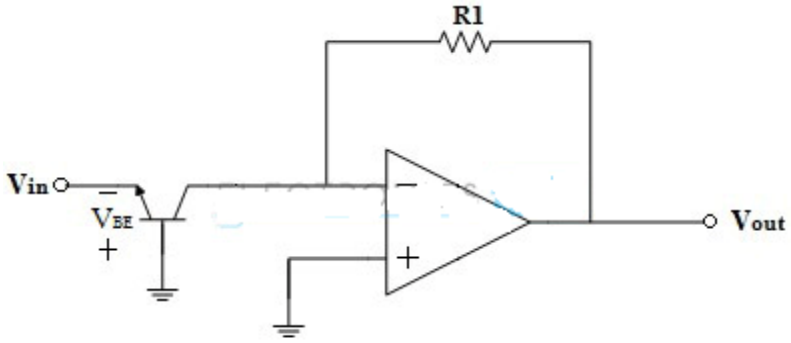


Fig: Anti-logarithmic Amplifier

It is noted that by exchanging the positions of the transistor and the resistor, the log amplifier can be made to work as antilog amplifier. The base-collector voltage of the transistor is maintained at ground potential, from the virtual ground concept. The current I_E for the transistor is given by,

$I_E = I_S.[e^{q(Vbe)/kT} – 1]$

For a grounded base transistor, $I_E = I_C$. Therefore,

$I_C = I_S.[e^{q(Vbe)/kT} – 1]$

Where, I_S = saturation current of the transistor,

$V_{out} = I_C.R_1$

$V_{out} = I_S.[e^{q(Vbe)/kT} – 1].R_1$

Also, for the above circuit $V_{in} = -V_{be}$. Therefore,

$V_{out} = R_1.I_S.[e^{q(-V_{in})/kT} – 1]$

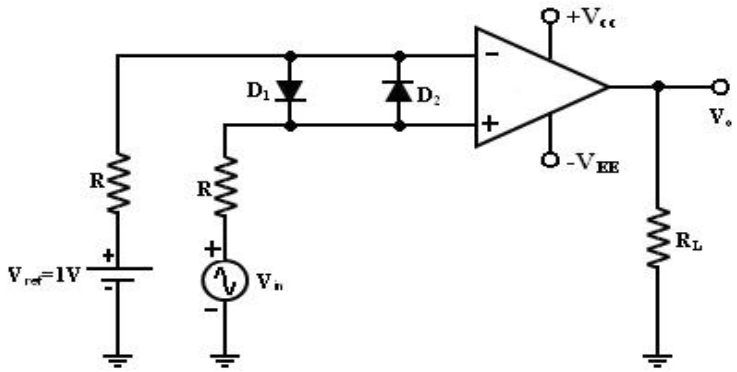
Antilog amplifiers also suffer from unstable outputs, due to the variations in I_S for different transistors and temperature dependence. Compensating circuits can be added to stabilize the output against such variations.

COMPARATOR

A comparator compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

- Digital Interfacing
- Schmitt Trigger
- Discriminator
- Voltage level detector and oscillators

Non-invertingComparator:



non-inverting comparator circuit

A fixed reference voltage V_{ref} of 1V is applied to the negative terminal and time varying signal voltage Vin is applied to the positive terminal.

When Vin is less than Vref the output becomes V_0 at –Vsat

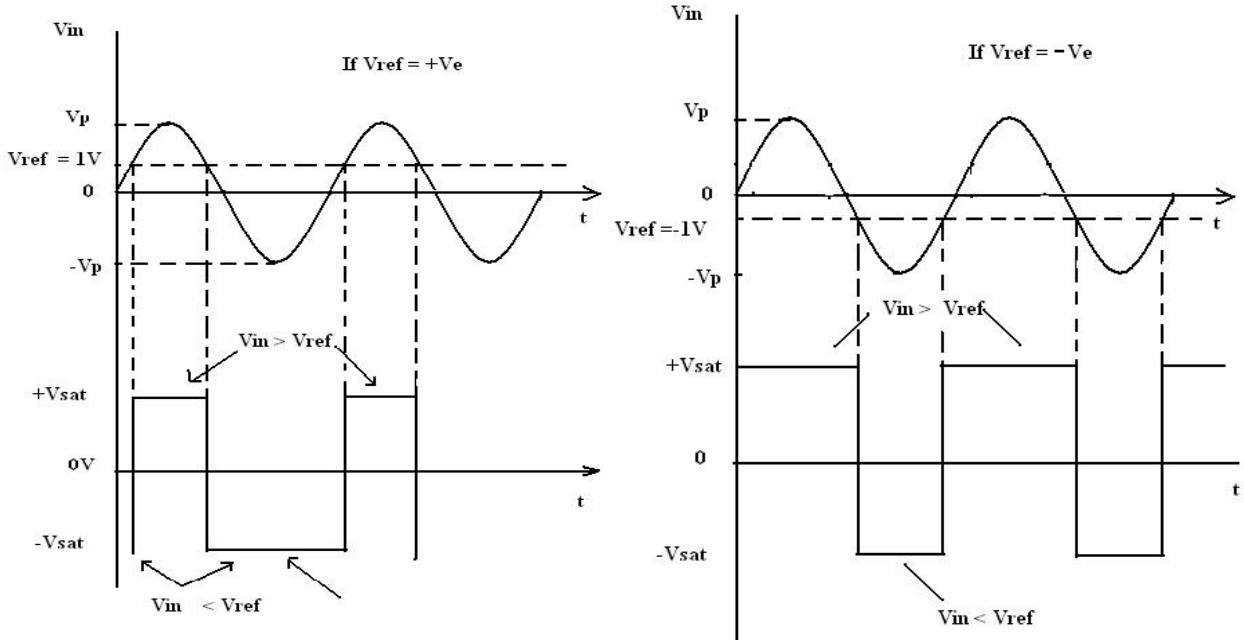
[Vin< Vref => V_0(-Vsat)].

When Vin is greater than Vref, the (+) input becomes positive, the V_0 goes to +Vsat.

[Vin > Vref => V_0 (+Vsat)].

Thus the V_0 changes from one saturation level to another.

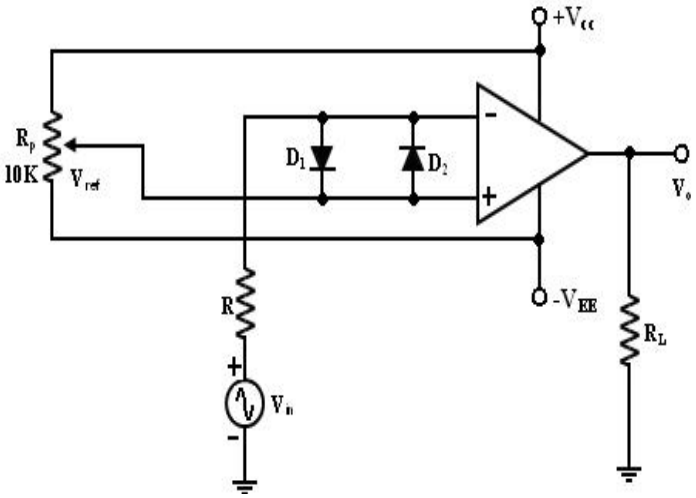
The diodes D_1 and D_2 protect the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes. The resistance Rin series with Vin is used to limit the current through $D_1$and D_2. To reduce offset problem ,a resistance Rcomp=R is connected between the (-ve) input and Vref.



Input and Output Waveforms of non-inverting comparator

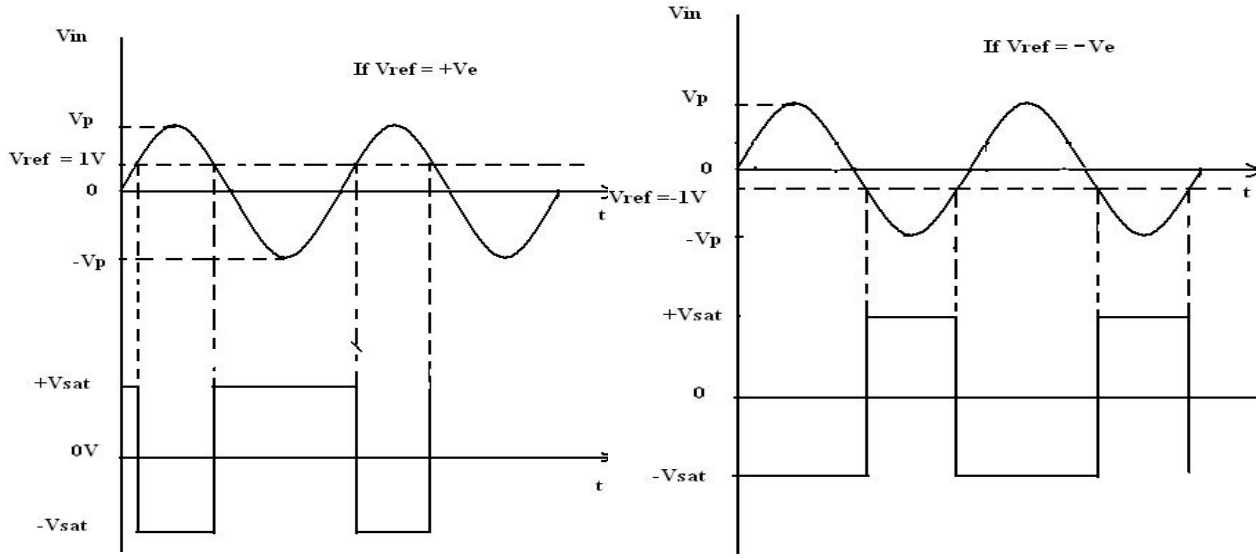
Inverting Comparator:

This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) Input terminal and Vin is applied to the (-) input terminal.



Inverting comparator circuit

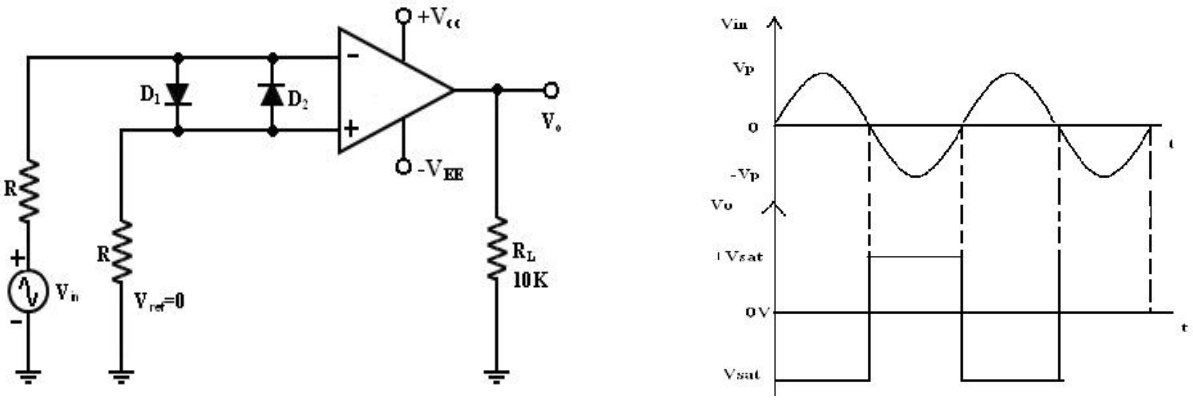
In this circuit Vref is obtained by using a 10K potentiometer that forms a voltage divider with DC supply volt +Vcc and -1 and the wiper connected to the input. As the wiper is moved towards +Vcc,Vref becomes more positive. Thus a Vref of a desired amplitude and polarity can be got by simply adjusting the 10kpotentiometer.



Input and Output Waveforms of non-inverting comparator

Applications:

Zero Crossing Detector:[Sine wave to Square wave converter]



Zero crossing detector circuit and input-output waveforms

One of the applications of comparator is the zero crossing detector or –sinewave to Square wave Converter. The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero.

This Fig shows when in what direction an input signal Vin crosses zero volts.(i.e.)the o/p V_0 is driven into negatives at duration when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.

Drawbacks of Zero-crossing detector:

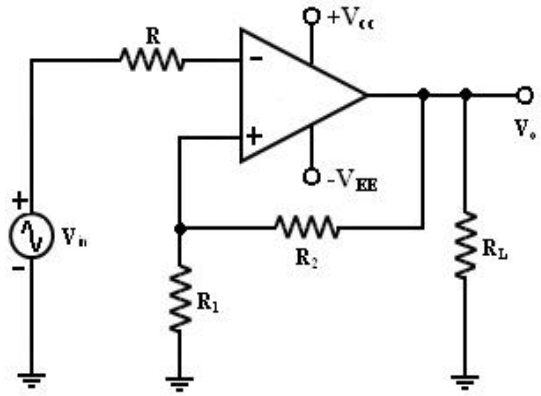
In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other.

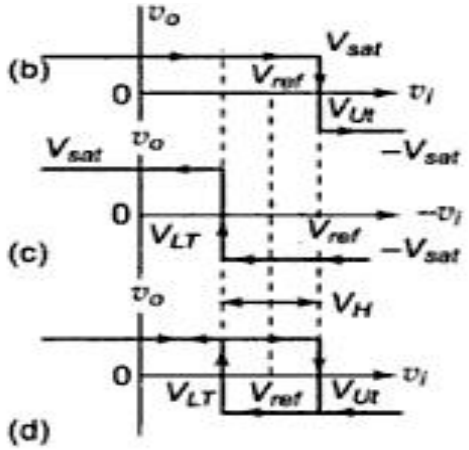
Because of the noise at the op-amp‘s input terminals the output V_0 may fluctuate between 2

saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V_0 to change faster an deliminate any false output transitions due to noise signals at the input Inverting comparator with positive feedback This is known as Schmitt Trigger.

SCHMITTTRIGGER:

This circuit converts an irregular shaped waveform to a square wave or pulse. The Circuit is known as Schmitt Trigger or squaring circuit. The input voltage Vin triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold voltage.





SchmittTriggercircuitandhysteresisphenomenon

These threshold voltages are obtained by using the voltage divider R_1–R_2, where the voltage across R_1 is feedback to the (+) input. The voltage across R_1 is variable reference threshold voltage that depends on the value of the output voltage. When V_0 = +Vsat, the voltage across R_1 is called upper threshold voltage Vut.

The input voltage Vin must be more positive than Vut in order to cause the output V_0 to switch from +Vsat to –Vsat using voltage divider rule,

Voltage at (+) input terminal is $V_{UT}=V_{ref}+R_2(V_{sat}-V_{ref})/(R_1+R_2)$ when $V_0=+V_{sat}$.

When $v_0=-V_{sat}$. Hysteris width $V_H=V_{UT}-V_{LT}=2R_2(V_{sat})/(R_1+R_2)$

When V_0 = -Vsat, the voltage across R_1 is called lower threshold voltage V_{lt}. The Vin must be more negative than V_{lt} in order to cause V_0 to switch from–Vsat to +Vsat.

for $V_{in}>V_{lt}$, V_0 is at –Vsat.

Voltage at(+)terminal is $V_{LT}=V_{ref}-R_2(V_{sat}+V_{ref})/(R_1+R_2)$.

- If the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions.
- Also the positive feedback, because of its regenerative action, will make V_0 switch faster

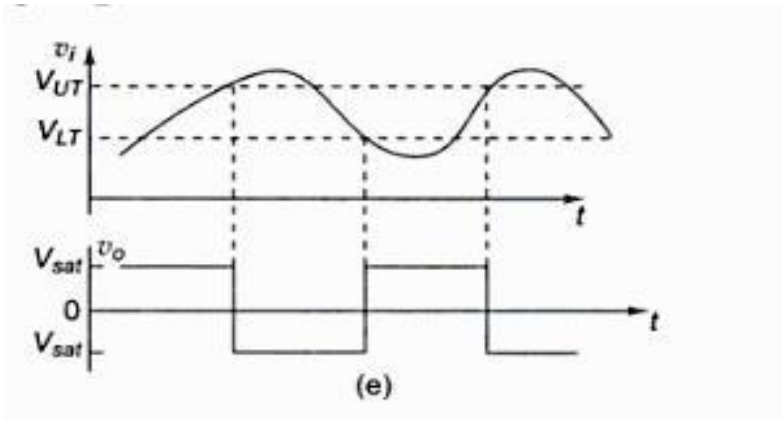
Between +Vsat and –Vsat.

- Resistance Rcomp =R1||R2 is used to minimize the offset problems.

The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds Vut its outputs witches from +Vsat to–Vsat and reverts to its original state, +Vsat when the input goes below V_{LT}. The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore

V_H = Vut–Vlt.

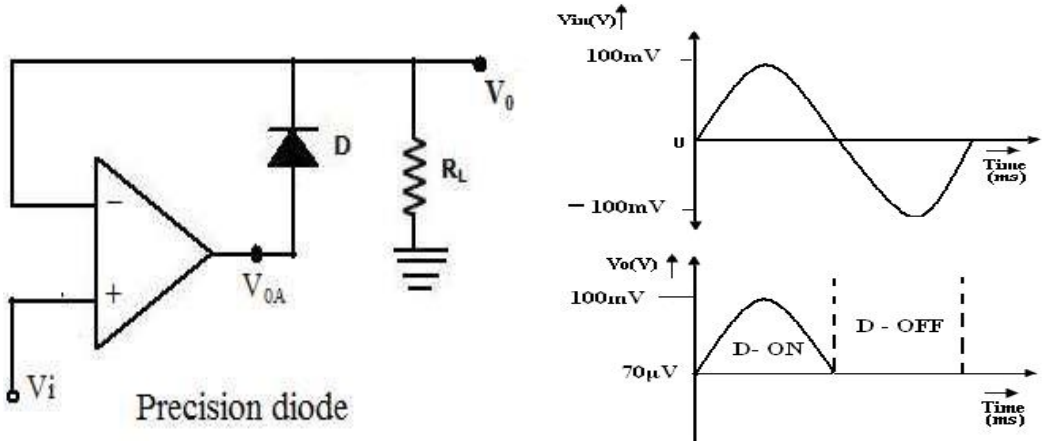
- If Vref=0,Vut=-V_{LT}=2R2(Vsat)/(R1+R2)



SchmittTriggerassquarer

PRECISIONRECTIFIER:

The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. Acircuit which can act as an ideal diode or precision signal–processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.



Precision diode and its waveform

Precisiondiodes:

Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half–wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage V_0=V_i.When V_i<0, the voltage V_{0A} becomes negative and

the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.

Consider the open loop gain A_{OL} of the op-amp is approximately 10^4 and the cut-in voltage V_γ for silicon diode is≈0.7V.When the input voltage $V_i > V_\gamma/A_{OL}$, the output of the op-amp V_{OA} exceeds V_γ and the diode D conducts.

Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma/A_{OL}$,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than 70μV as shown in figure.

When V_i is negative or less than V_γ / A_{OL}, the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus $V_0=0$.

No current is then delivered to the load $R_L$except for the small bias current of the op-amp And the reverse saturation current of thediode.

This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region($V_i<0$). Since the output swings to negative saturation level when $V_i<0$, the circuit is basically of saturating form. Thus the frequency response is also limited.

Applications:

The precision diodes are used in
Half wave rectifier,
Full-wave rectifier,
Peak value detector,
Clipper and clamper circuits

Disadvantage:

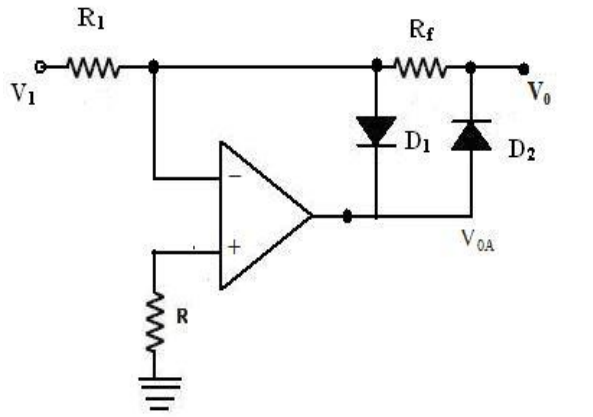
It can be observed that the precision diode as shown in figure operated in the first quadrant with $V_i > 0$ and $V_0 > 0$. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

Half–wave Rectifier:

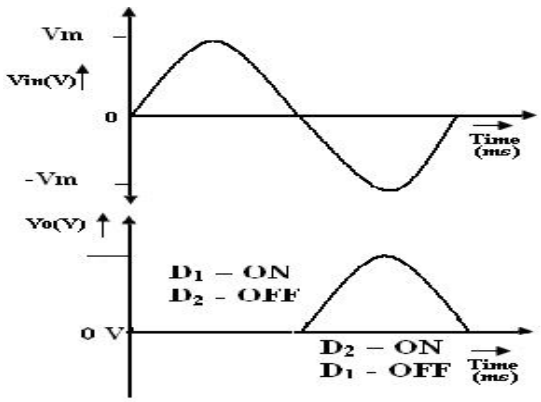
A non-saturating half wave precision rectifier circuit is shown in figure. When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative.

This results in forward biasing the diode D_1 and the op-amp output drops only by≈0.7V below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive.

When $V_i>0$, the op-amp output V_{OA} becomes positive, forward biasing the diode $D_2$and reverse biasing the diode D_1. The circuit then acts like an inverting amplifier circuit with an on-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.



Non - Saturating half - wave precision rectifier circuit



Input and Output Waveforms

Halfwaverectifieranditsoperation

Thecircuitoperationcanmathematicallybeexpressedas

$V_0=0$ when $V_i>0$and

$V_0=R_f/R_iV_1$ for$V_i<0$

The voltage V_{OA} at the opamp output is V_{OA}= -0.7V for $V_i>0$

$V_{OA}=R_f/R_iV_1+0.7V$ for$V_{i<0}$

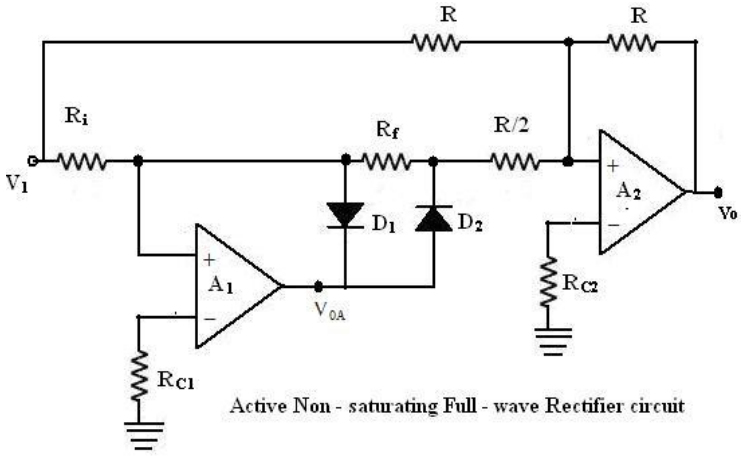
Advantages:

- It is a precision half wave rectifier and
- It is an on saturating one.

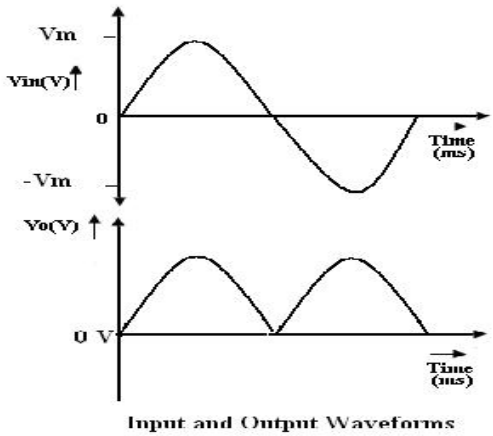
The inverting characteristics of the output V_0 can be circumvented by the use of an additional inversion for achieving a positive output.

2.15.2FullwaveRectifier:

The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier.



Active Non - saturating Full - wave Rectifier circuit



Input and Output Waveforms

Full wave rectifier and its operation

For positive input voltage $V_i>0$Vandassuming that $R_F=R_i=R$, the output voltage $V_{OA}=V_i$. The voltage

V_0 appears as(-) in put to the summing op-amp circuit formed by A_2,The gain for the input V_0 is R/(R/2), as shown in figure.

The input V_i also appears as an input to the summing amplifier. Then, the net output is

$V_0 = -V_i - 2V_0 = -V_i - 2(-V_i) = V_i$. Since $V_i > 0V$, V_0 will be positive, with its input output Characteristics in first quadrant. For negative input $V_i < 0V$, the output V_0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero.

However, V_i is also applied as an input to the summer circuit formed by the op-amp A_2.

The gain for this input id(-R/R)=-1,and hence the output is $V_0 = -V_i$. Since V_i is negative, V_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.

To summarize the operation of the circuit,

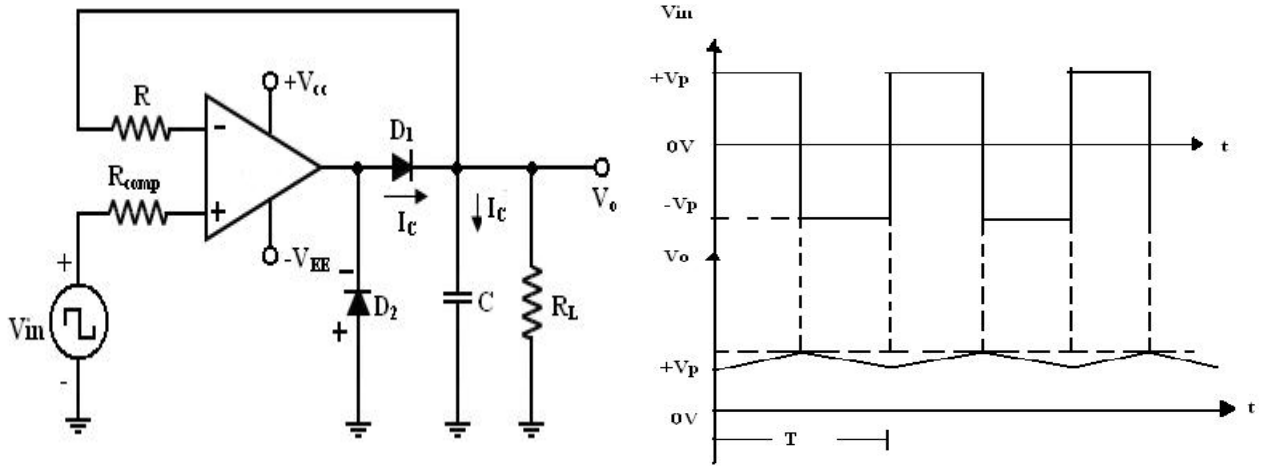
$V_0 = V_i$ when $V_i < 0V$and

$V_0 = V_i$ for $V_i > 0V$,and hence

$V_0 = |V_i|$

PEAK DETECTOR

Square, Triangular, Sawtooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional AC voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the RMS value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.



Peak detector circuit and input and output waveforms

i)During the positive half cycle of Vin:

the o/pof the op-amp drives D_1 on.(Forwardbiased)

Charging capacitor C to the positive peak value V_p of the input volt Vin.

ii)During the negative half cycle of Vin:

D_1 is reverse biased and voltage across C is retained.

The only discharge path for C is through R_L since the input bias I_B is negligible.

For proper operation of the circuit, the charging time constant(CR_d) and discharging time constant

(CR_L) must satisfy the following condition.

$CR_d <= T/10$

Where R_d = Resistance of the forward – biased diode.

T= time period of the input waveform.

$CR_L >= 10T$ (2)

Where R_L= load resistor.

If R_L is very small so that eqn.(2)cannot be satisfied.

- Usea (buffer)voltage follower circuit between capacitor C and R_L load resistor.
- R is used to protect the op-amp against the excessive is charge currents.
- Rcomp = minimizes the offset problems caused by input current
- D_2 conducts during the –ve halfcycle of Vin and prevents the op-amp from going into Negative saturation.

Note: -ve peak of the input signal can be detected simply by reversing diode D_1 and D_2

CLIPPER AND CLIPPER

Applications:

Wave shaping circuits are commonly used in digital computers and communication such as TV and FM receiver.

Wave shaping technique include clipping and clamping.

In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform.

The diode works as an ideal diode (switch) because when on, the voltage drop across the diode is divided by the open loop gain of the op-amp. When off(reverse biased)the diode is an open circuit. In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is some times called a dc inverter.

2.17.1 Positive and Negative

Clipper: Positive Clipper:

A circuit that removes positive parts of the input signal can be formed by using an op-amp with a Rectifier diode. The clipping level is determined by the reference voltage Vref, which should less than the i/p range of the op-amp ($V_{ref} < V_{in}$). The Output voltage has the portions of the positive half cycles above V_{ref} clipped off.

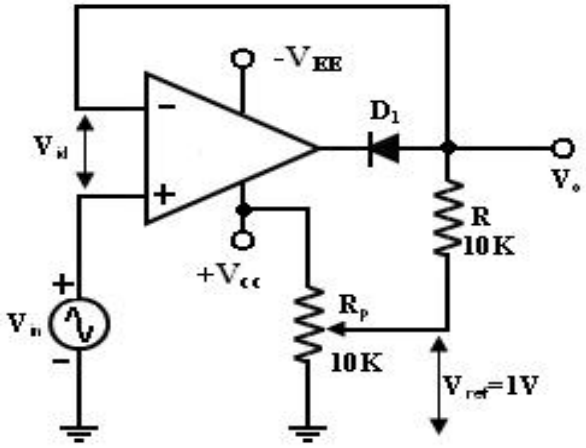
The circuit works as follows:

During the positive half cycle of the input, the diode D_1 conducts only until Vin = Vref. This happens because when Vin < Vref, the output volts V_0 of the op-amp becomes negative to device D_1 into conduction when D_1 conducts it closes feedback loop and op-amp operates as a voltage follower.(i.e.) Output V_0 follows input until Vin = Vref.

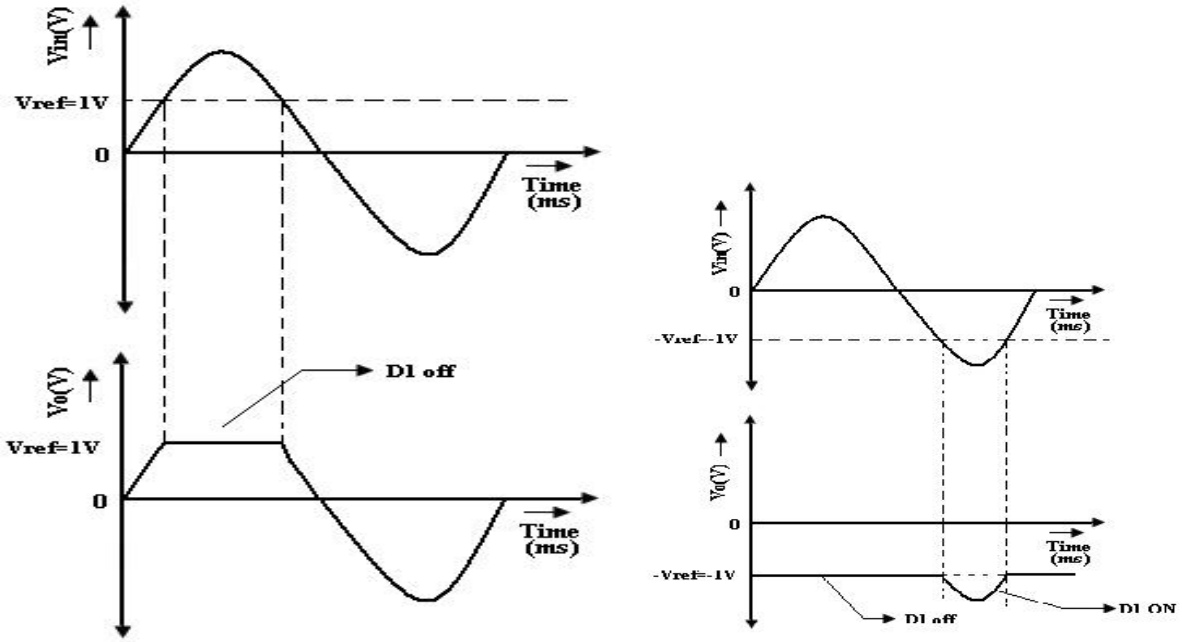
When Vin > Vref => the V_0 becomes +ve to derive D_1 into off. It opens the feedback loop and op-amp operates open loop. When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V_0 again becomes –ve to device D_1 into conduction. It closes the feedback path. (o/p follows the i/p). Thus diode D_1 is on for vin < Vref (o/p follows the i/p) and D_1 is off for Vin > Vref.

The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably

compensated for unity gain.



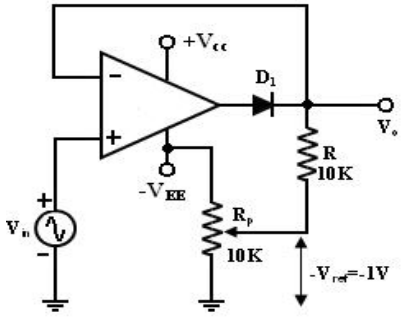
Positive Clipper



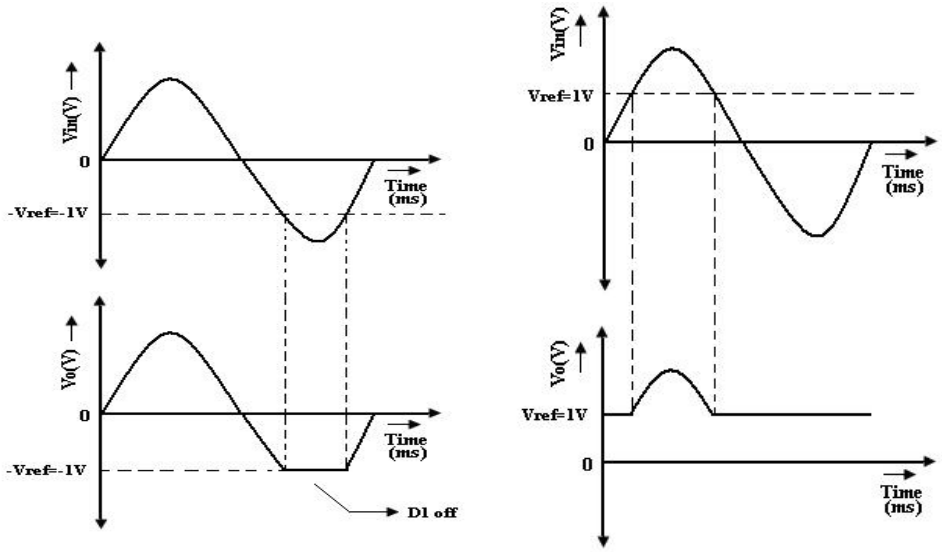
Positive clipper input output waveforms

Ex: for high speed op-amp HA2500, LM310, μA318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D_1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If R_P(pot)is connected to– V_{EE} instead of +Vcc, the ref voltage Vref will be negative (Vref=-ve). This will cause the entire o/p waveform above –Vref to be clipped off.

NegativeClipper:



Negativeclipper



Input output waveforms

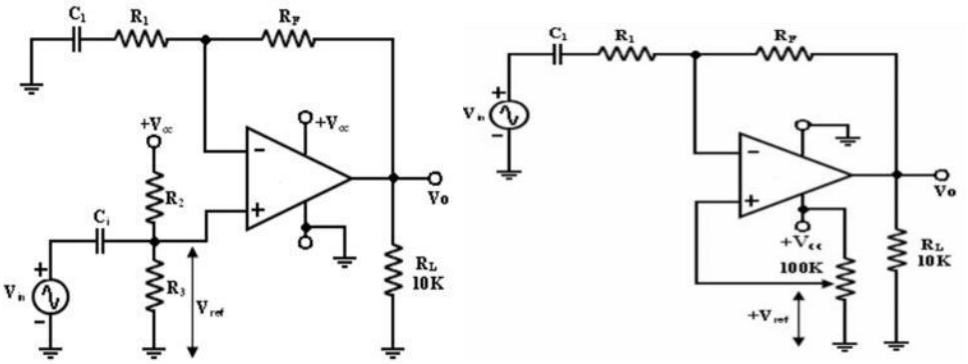
The positive clipper is converted into a –ve clipper by simply reversing diode D_1 and changing the polarity of Vref voltage. The negative clipper clips off the –ve parts of the input signal below the reference voltage. Diode D_1 conducts -> when Vin >- Vref and therefore during this period o/p volt V_0 follows the i/p volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D_1 is off) Vin < -Vref. If –Vref is changed to –Vref by connecting the potentiometer R_P to the +Vcc, the V_0 below +Vref will be clipped off. The diode D_1 must be on for Vin > Vref and off or Vin.

Positive and Negative Clampers:

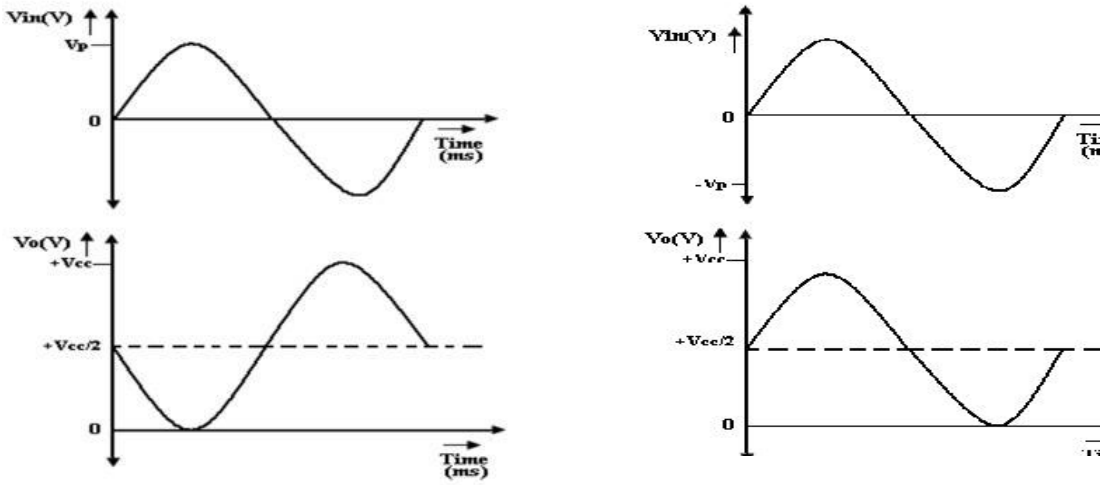
In clamper circuits a predetermined dc level is added to the output voltage.(or) The output is clamped to a desired dc level.

1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that uses this technique.



Positive – Negative clampers



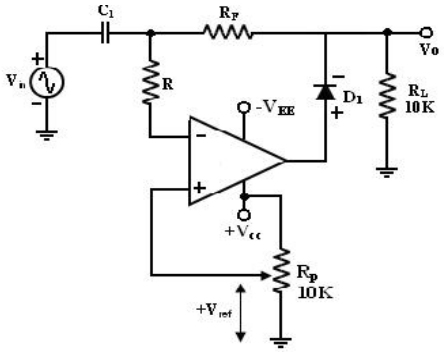
Input and output waveform with +Vref

Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

1. In both circuits the dc level added to the o/p voltage is approximately equal to Vcc/2.
2. This +ve fixed dc level is needed to obtain a maximum undistorted symmetrical sine wave.

Peak clamper circuit:

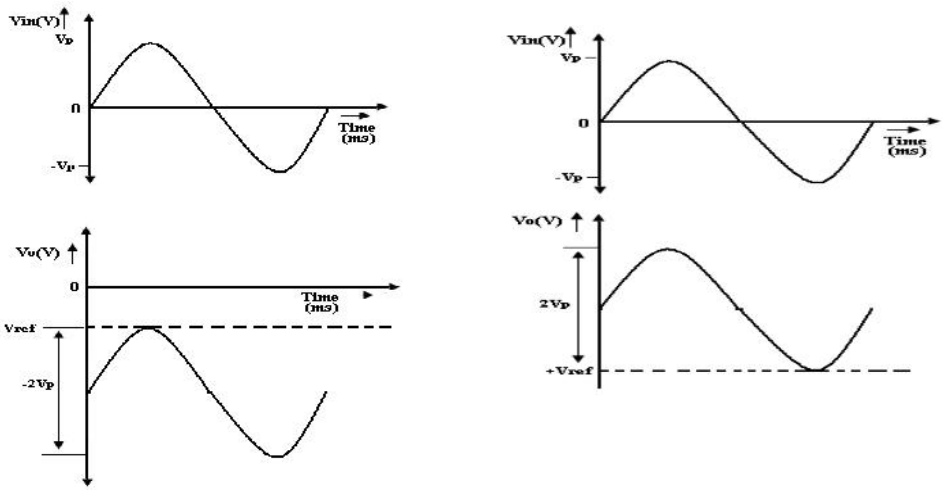


Peak clamper circuit

In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.

First consider the input voltage Vref at the (+) input: since this volt is +ve, V_0 is also +ve which forward biases D_1.This closed the feedback loop.

Voltage Vin at the (-) input: During its –ve half cycle, diode D_1 conducts, charging c; to the -ve peak value of V_p. During the +ve half cycle, diode D_1 in reverse biased. Since this voltage V_p is in series with the +ve peak volt V_p the o/p volt $V_0=2V_p$. Thus the net to/pisVref plus $2V_p$. So the –ve peak of 2 V_p is at Vref. For precision clamping, $C_iR_d<<T/2$



Input and Output Waveform with –Vref

Where R_d = resistance of diode D_1 when it is forward biased.

T=time period of the input waveform.

Resistor R is used to protect the opamp against excessive discharge currents from capacitor C_i especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by

Reversing D_1 and using –ve referencevoltage (-Vref).

N o t e :

InvandNon-Invclamper–

Fixeddclevel

Peakclamper–

Variabledclevel

ACTIVE FILTERS

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band.

Filters may be classified as

1. Analog or digital.
2. Active or passive
3. Audio(AF) or Radio Frequency(RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals Using digital technique.

2.Activeor Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

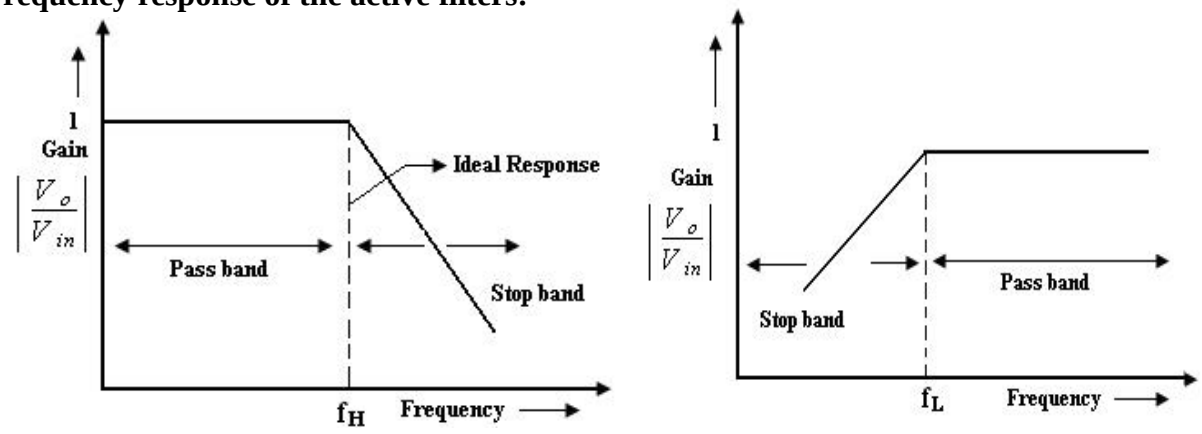
Active filters offer the following advantages over passive filters:

1. Gain and Frequency adjustment flexibility:
   Since the op-amp is capable of providing gain, the i/p signal is not attenuated as it is in a passive filter.[Active filter is easier to tune or adjust].
2. No loading problem:
   Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.
3. Cost:
   Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

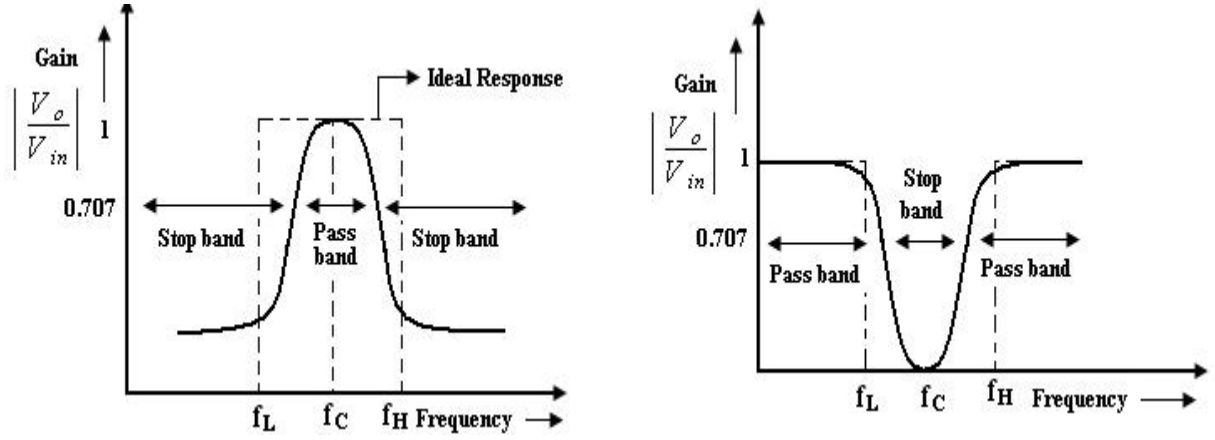
 The most commonly used filters are these:

1. Low pass Filters
2. High pass Filters
3. Band pass filters
4. Band–reject filters
5. All pass filters.

Frequency response of the active filters:



Frequency response of Low Pass filter and High pass Filter



Frequency response of Band Pass filter and Band reject Filter

The rate at which the gain of the filter changes in the stop band is determined by the order of the filter.

Ex: 1st order low pass filter the gain rolls off at the rate of 20dB/decade in the stop band. (i.e) for $f>f_H$.

2nd order LPF->the gain roll off rate is 40dB/decade.

1st order HPF->the gain rolls off at the rate of 20dB(i.e.) until f:fL
2ndorderHPF ->the gain rolls off at the rate of 40dB/decade

First order LPF Butterworth filter:

First order LPF that uses an RC for filtering op-amp is used in the non-inverting configuration. Resistor R1&Rf determine the gain of the filter. According to the voltage–divider rule, the voltage at the non-inverting terminal (across capacitor)C is,

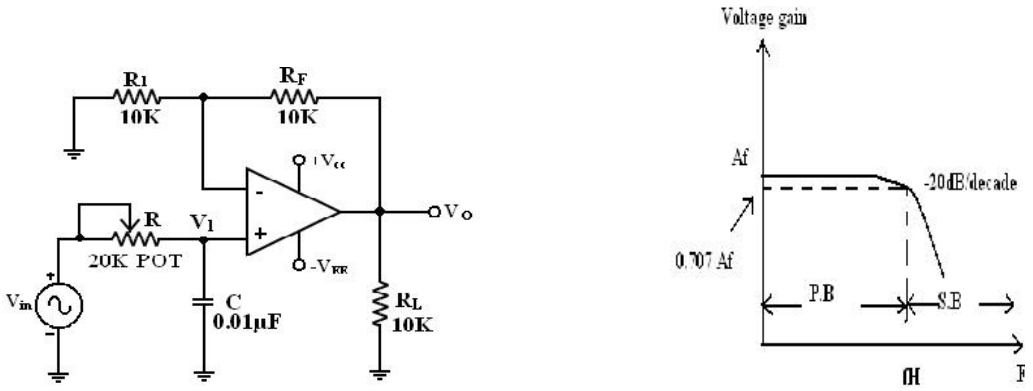


Fig.2.54FirstorderLPFButterworthfilter

GainA=(1+Rf/R1)

Voltage across capacitor

$V_1=V_i/(1+j2\pi fRC)$

Output voltage V0 for non inverting amplifier $=AV_1 = (1+R_f/R_1)V_i/(1+j2\pi fRC)$

Overall gain $V_0/V_i=(1+R_f/R_1)V_i/(1+j2\pi fRC$

Transfer function $H(s)=A/(jf/f_h+1)$ if $f_h=1/2\pi RC$

$H(j\omega)=A/(j\ RC+1)=A/(j\ RC+1)$.

The gain magnitude and phase angle of the equation of the LPF can be obtained by Converting eqn.(1)bin to its equivalent polar form as follows.

1.At very low frequency, $f< f_H$

$|H(j\omega)|=A$

2. $Atf=f_H$

$|H(j\omega)|=A/\sqrt{2}=0.707A$

3. $Atf>f_H$

$|H(j\omega)|<<A\cong 0$

When the frequency increases by tenfold (one decade), the volt gain is divided by 10.The gain falls by 20dB(=20log10) each time the frequency is reduces by 10. Hence the rate at which the gain rolls off f_H=20dBor6dB/octave(two fold Rin frequency). The frequency $f=f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3dB(=20log0.707).

Filter design:

A LPF can be designed by implementing the following steps.

1.Choose a value of high cut off frequency f_H.

2.Select a value of C less than or equal to 1μf.

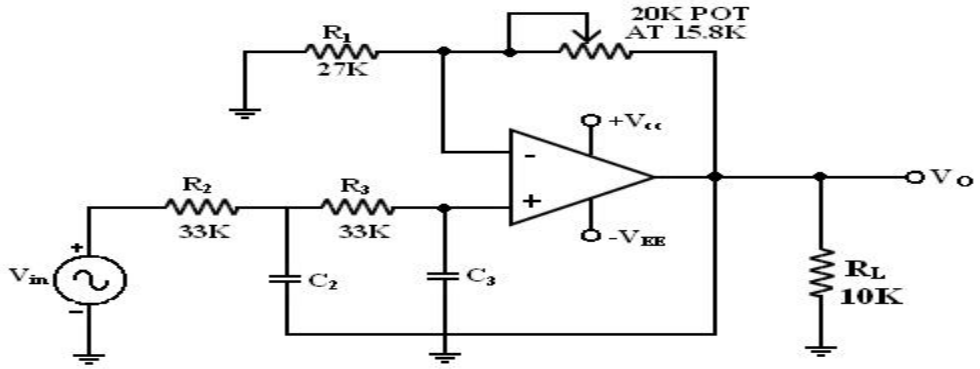
3.Choose the value of R using $f_h=1/2\pi RC$

4.Finally select values of R1 and RF dependent on the desired pass band gain AF Using A=(1+Rf/R1)

Second order LP Butterworth filter:

A second order LPF having a gain 40dB/decade in stopband. A First order LPF can be converted into a II order type simply by using an additional RC network.

The gain of the II order filter is set byR1 and R_F, while the high cut off frequency f_H is determined by R2, C2, R3 andC3.



Second order LP Butterworth filter

Let $Y_1 = Y_2 = 1/R$, $Y_3 = sC_3$ and $Y_4 = sC_4$. Then the transfer function is

$$H(s) = \frac{\frac{1}{R^2}}{\frac{1}{R^2} + sC_4\left(\frac{2}{R} + sC_3\right)} = \frac{1}{1 + sRC_4(2 + sRC_3)}$$

Let the time constant $\tau_1 = RC_3$ and $\tau_2 = RC_4$. Substituting $s = j\omega$, we get

$$H(j\omega) = \frac{1}{1 + j\omega\tau_2(2 + j\omega\tau_1)} = \frac{1}{(1 - \omega^2\tau_1) + j(2\omega\tau_2)}$$

Therefore, its magnitude is

$$|H(j\omega)| = \left[(1 - \omega^2\tau_1\tau_2)^2 + (2\omega\tau_2)^2\right]^{-1/2}$$

A maximally flat Butterworth filter will have a minimum rate of change. Therefore,

$$\frac{d|H|}{d\omega}\Big|_{\omega=0} = 0$$

Differentiating $|H(j\omega)|$, we obtain

$$\frac{d|H|}{d\omega} = -\frac{1}{2}\left[(1 - \omega^2\tau_1\tau_2)^2 + (2\omega\tau_2)^2\right]^{-3/2}\left[-4\omega\tau_1\tau_2(1 - \omega^2\tau_1\tau_2) + 8\omega\tau_2^2\right]$$

Letting the derivative to zero at $\omega = 0$, we get

$$\frac{d|H|}{d\omega}\Big|_{\omega=0} = \left[-4\omega\tau_1\tau_2(1 - \omega^2\tau_1\tau_2) + 8\omega\tau_2^2\right]$$

$$= 4\omega\tau_2\left[-\tau_1(1 - \omega^2\tau_1\tau_2) + 2\tau_2\right]$$

The above equation is satisfied when $2\tau_2 = \tau_1$. That is, $C_3 = 2C_4$. Therefore the magnitude of the transfer function becomes

$$|H| = \frac{1}{\left[1 + 4(\omega\tau_2)^4\right]^{1/2}}$$

The cut-off frequency occurs when $|H| = \frac{1}{\sqrt{2}}$, or $4(\omega_{3dB}\tau_2)^4 = 1$. Therefore,

$$\omega_{3dB} = 2\pi f_{3dB} = \frac{1}{\tau_2\sqrt{2}} = \frac{1}{\sqrt{2}RC_4}$$

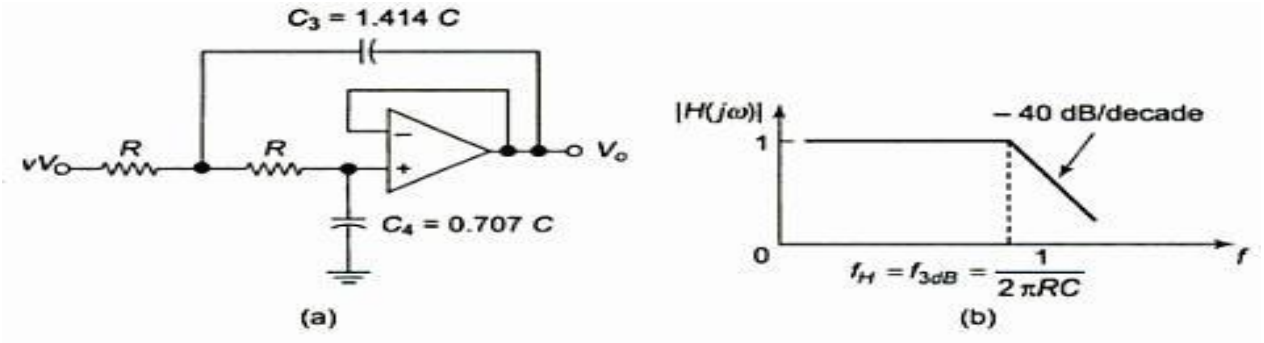
We know that the cut-off frequency is $\omega_H = \omega_{3dB} = \frac{1}{RC}$.

Comparing the above equations, we get

$$C_4 = 0.707C$$

$$C_3 = 1.414C$$

The magnitude of the voltage transfer function for the second order low-pass Butterworth filter is $|H(jf)| = \frac{1}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$



Second order Low pass Butterworth and filter with unity gain and its transfer

function

Filter Design:

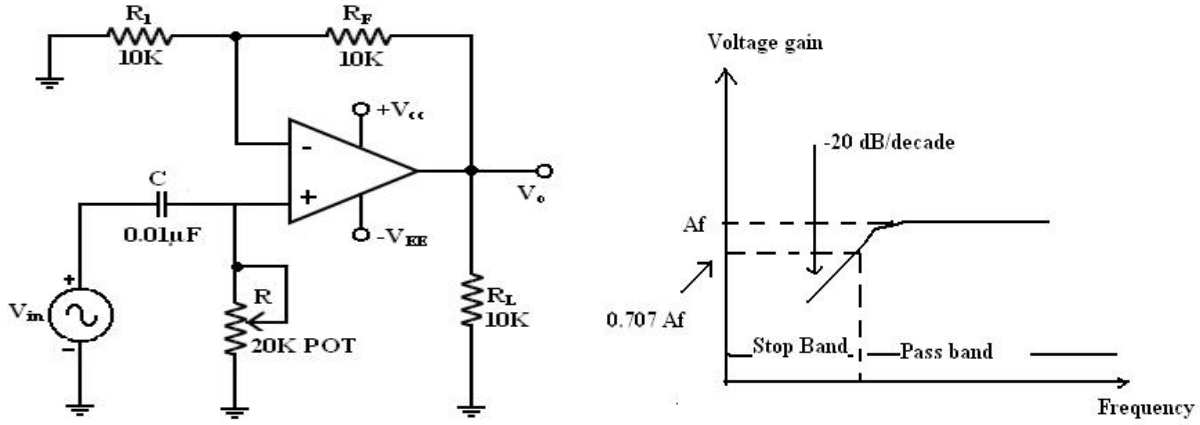
1. Choose a value for a high cut off freq.(f_H).
2. To simplify the design calculations, set $R_2=R_3=R$ and $C_2=C_3=C$ then choose a value of $C<=1\mu f$.
3. Calculate the value of R $R=1/2\pi f_h C$
4. Finally, because of the equal resistor ($R_2=R_3$) and capacitor ($C_2=C_3$)values, the pass band volt gain $A_F=1+R_F/R_1$of these cond order had to be=to1.586. $R_F=0.586$ R_1.Hence choose a value of $R_1<=100k\Omega$.

5. Calculate the value of R_F.

First order HP Butterworth filter:

High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low – pass filters.

(i.e) I order HPF is formed from a I order LPF by interchanging components R &C. Similarly II order HPF is formed from a II order LPF by interchanging R&C.



I order HPF and its frequency response

Here I order HPF with a low cut off frequency off$_L$. This is the frequency at which the magnitudeofthegainis0.707timesitspassbandvalue.

Here all the frequencies higher than f_L are pass band frequencies.

TheoutputvoltageV0of the first order active high pass filter is

$$V_o=\left(1+\frac{R_f}{R_i}\right)\frac{j2\pi fRC}{1+j2\pi fRC}V_i$$

The gain of the filter:

$$\frac{V_o}{V_i}=A\left(\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right)$$

Frequency response of the filter $|H(jf)|=\left|\frac{V_o}{V_i}\right|=\frac{A\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}}=\frac{A}{\sqrt{1+\left(\frac{f_L}{f}\right)^2}}$ is

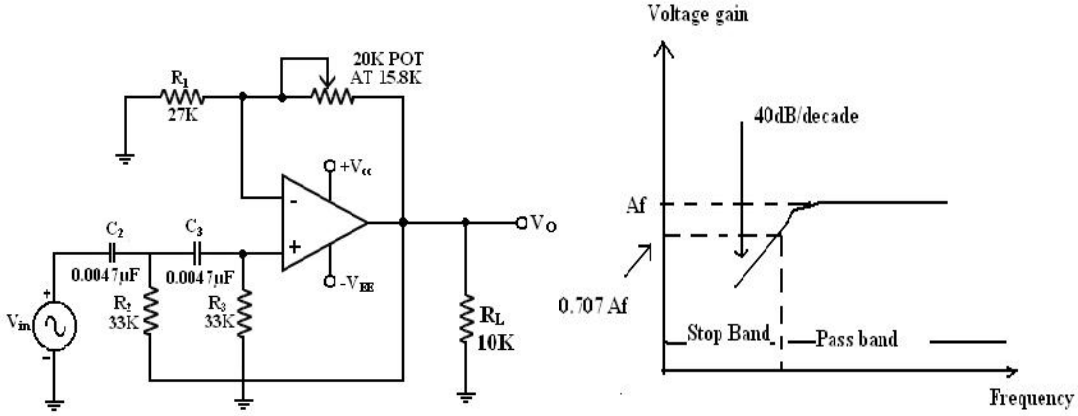
At high frequencies f>fL gain=A.

At f=fL gain=0.707A.

At f<fL the gain decreases at a rate of -20 db/decade. The frequency below cutoff frequency is stop band.

Second–order High Pass Butterworth Filter:

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency



II order HPF and its frequency response

Band pass filters

Filters that pass band of frequencies and attenuates others. Its high cutoff frequency and low cut off frequency are related as $f_H > f_L$ and maximum gain at resonant frequency $f_r = \sqrt{f_H f_L}$

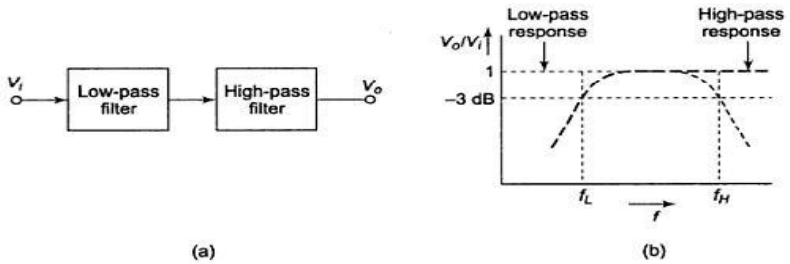
Figure of merit $Q = f_r/(f_H - f_L) = f_r/B$ where B=bandwidth.

2 types of filters are Narrow band pass and wide band pass filters

Wide band pass filter:

It is connection of a low pass filter and a high pass filter in cascade.

The f_H of low pass filter and f_L of high pass filter are related as $f_H > f_L$



(a)Wide band pass filter and (b) its frequency response

UNIT III
ANALOG MULTIPLIER AND PLL

Analog Multipliers:

A multiple produces an output V0 which is proportional to the product of two inputs Vx And Vy. V0 = KVxVy where K is the scaling factor = (1/10) V^{-1}.

There are various methods available for performing analog multiplication. Four of such techniques, namely,

1. Logarithmic summing technique
2. Pulse height/width modulation Technique
3. Variable trans conductance Technique
4. Multiplication using Gilbert cell and

Multiplication using variable trans conductance technique

$$V_0 = \frac{(V_x + \phi_x)(V_y + \phi_y)}{10(1+\varepsilon)} + \phi_0$$

where φx and φy are the offsets associated with signals Vx and Vy, ε is the error signal associated with K and φ0 is the offset voltage of the multiplier output.

Terminologies associated voltage of the multiplier characteristics:

- **Accuracy:**

This specifies the derivation of the actual output from the ideal output, for any combination of X and Y inputs falling within the permissible operating range of the multiplier.

- **Linearity:**

This defines the accuracy of the multiplier. The Linearity Error can be defined as the maximum absolute derivation of the error surface. This linearity error imposes a lower limit on the multiplier accuracy.

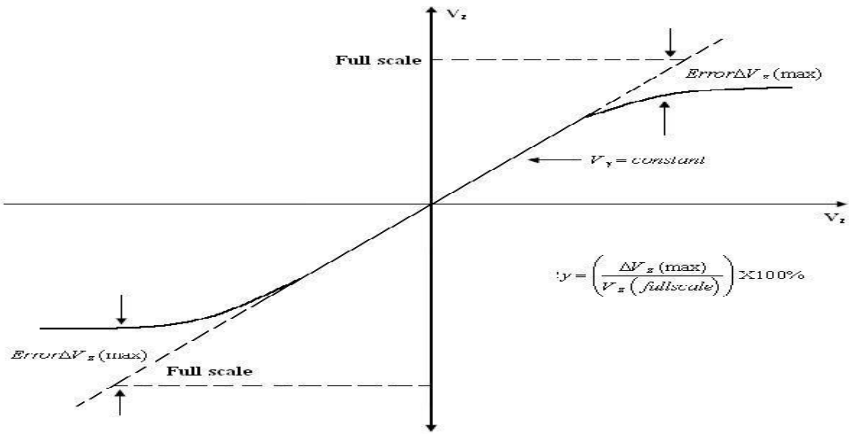


Fig.3.1 Linearity of the multiplier

The figure shows the response of the output as a function of one input voltage Vx when the other Vy is assumed constant. It represents the maximum percentage derivation from the ideal straight line output. An error surface is formed by plotting the output for different combinations of X and Y inputs.

- **Square law accuracy:**

The Square – law curve is obtained with the X and Y inputs connected together and applied with the same input signal. The maximum derivation of the output voltage from an ideal square –law curve expresses the squaring mode accuracy.

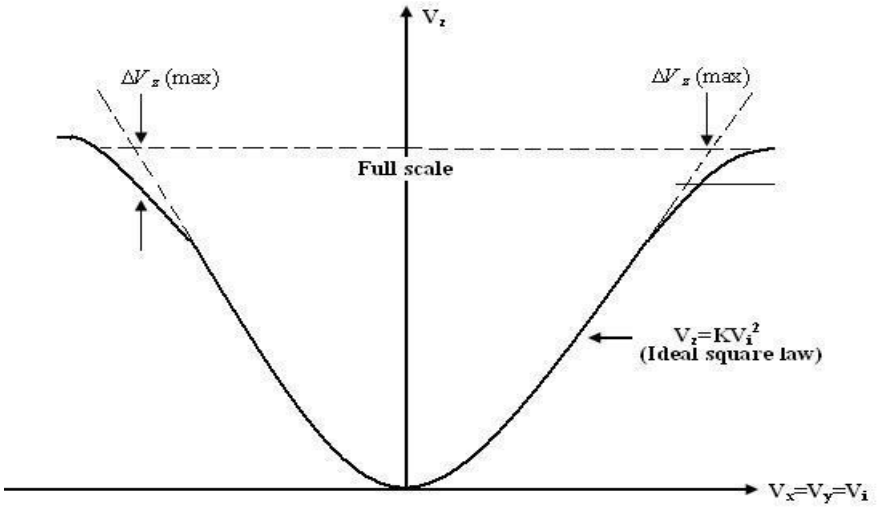


Fig. 3.2 squaring mode accuracy

- **Bandwidth:**

The Bandwidth indicates the operating capability of an analog multiplier at higher frequency values. Small signal 3 dB bandwidth defines the frequency f0 at which the output reduces by 3dB from its low frequency value for a constant input voltage. This is identified individually for the X and Y input channels normally.

The transconductance bandwidth represents the frequency at which the transconductance of the multiplier drops by 3dB of its low frequency value. This characteristic defines the application frequency ranges when used for phase detection or AM detection.

- **Quadrant:**

The quadrant defines the applicability of the circuit for bipolar signals at its inputs. First – quadrant device accepts only positive input signals, the two quadrant device accepts one bipolar signal and one unipolar signal and the four quadrant device accepts two bipolar signals.

- **Logarithmic summing Technique:**

This technique uses the relationship lnVx + lnVy =ln(VxVy)

As shown in figure the input voltages Vx and Vy are converted to their logarithmic equivalent, are then added together by a summer.An antilogarithmic converter which produces the output voltage of the summer.The output is given by,

$Vz = \ln^{-1} (\ln(VxVy)) = VxVy$

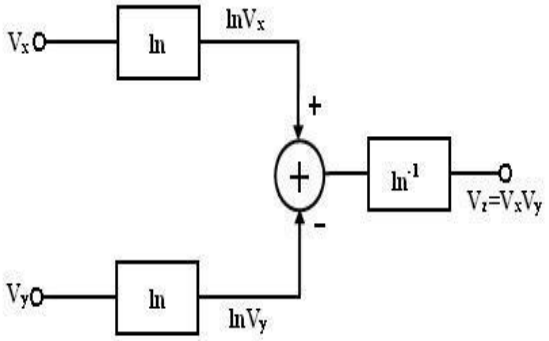


Fig. 3.3 logarithmic summing method

The relationship between I0 and VBE of the transistor is given by

$$IC = I0e^{(VBE/VT)}.$$

It is found that the transistor follows the relationship very accurately in the range of 10nA to 100mA. Logarithmic multiplier has low accuracy and high temperature instability. This method is applicable only to positive values of Vx and Vy.

Limitation: this type of multiplier is restricted to one quadrant operation only.

- **Pulse Height/ Width Modulation Technique:**

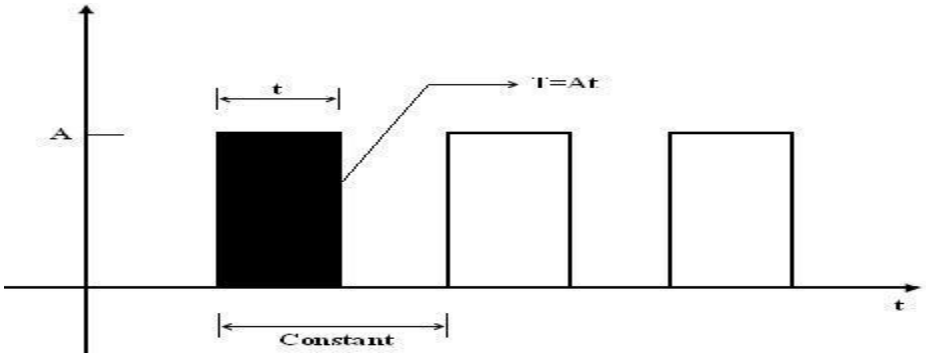


Fig.3.4 Pulse Height/ Width Modulation Technique

In this method, the pulse width of a pulse train is made proportional to one input voltage and the pulse amplitude is made proportional to the second input voltage. Therefore, Vx =Kx A, Vy =Ky t, and Vz =Kz T where Kx, Ky, Kz are scaling factors. In figure A is the amplitude of the pulse, t is the pulse width and T is the area ofthe pulse.

Therefore,

$$V_z = K_z T = \frac{V_x V_y}{k_x k_y}$$

The modulated pulse train is passed through an integrated circuit. Therefore, the input of the integrator is proportional to the area of pulse, which in turn is proportional to the product of two input voltages.

3.1 Analog multiplier using an Emitter coupled Transistor pair:

The output currents IC1 an d IC2 are related to the differential input voltage V1 by

$$I_{C1} = \frac{I_{EE}}{1+e^{V_1/V_T}} \text{ and } I_{C2} = \frac{I_{EE}}{1+e^{V_2/V_T}}$$

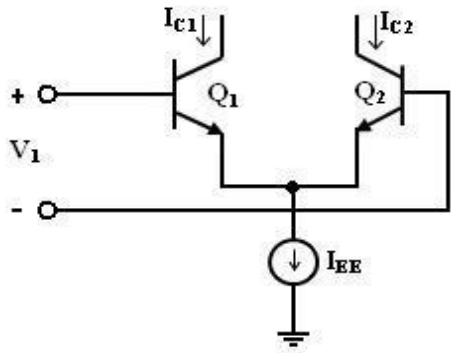


Fig.3.5 multiplier circuit using an emitter coupled pair

Where V i s thermal voltage and the base currents have been neglected. Combining above eqn. difference betweenthe two output currents as

$$\Delta IC = IC1 - I\,C = \frac{I_{EE}}{1+e^{v1/vT}} - \frac{I_{EE}}{1+e^{v2/vT}} = I\,EE\tanh\,(V1/2VT)$$

The dc transfer characteristics of the emitter – coupled pair is shown in figure. It shows that the emitter coupled pair can be used as a simple multiplier using this configuration. When the differential input voltage V1 << VT, we can appropriate as given by

$\Delta IC = I\,EE\,(V1/2VT)$

The current I_{EE} is the bias current for the emitter – coupled pair. If the current I_{EE} is made proportional to a second input signal V2, then

$$I_{EE} = K\ 0\ V1\ (V2 - V\ BE)/2VT$$

Substituting above eqn., we get $\Delta IC = K\ 0\ V1\ (V2 - V\ BE)/2VT$

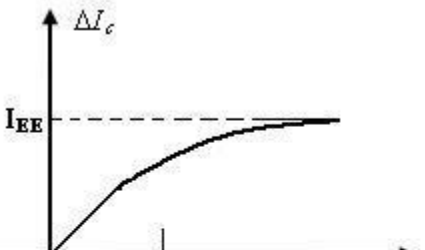


Fig. 3.6 DC Transfer characteristics of emitter coupled pair

This arrangement is shown in figure. It is a simple modulator circuit constructed using a differential amplifier. It can be used as a multiplier, provided V1 is small and much less than 50mV and V2 is greater than VBE (on). But, the multiplier circuit shown in figure has several limitations. The first limitation is that V2 is offset by VBE (on).

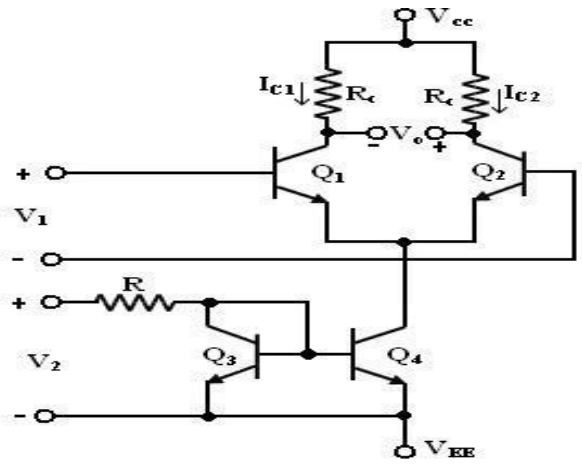


Fig. 3.7 A simple modulator using a differential amplifier

The second is that V2 must always be positive which results in only a two-quadrant multiplier operation. The third limitation is that, the tanh (X) is approximately as X, where X = V1 /2VT. The first two limitations are overcome in the Gilbert cell.

3.2 Gilbert Multiplier cell:

The Gilbert multiplier cell is a modification of the emitter coupled cell and this allows four – quadrant multiplication. Therefore, it forms the basis of most of the integrated circuit balanced

Multipliers. Two cross- coupled emitter- coupled pairs in series connection with an emitter coupled pair form the structure of the Gilbert multiplier cell.

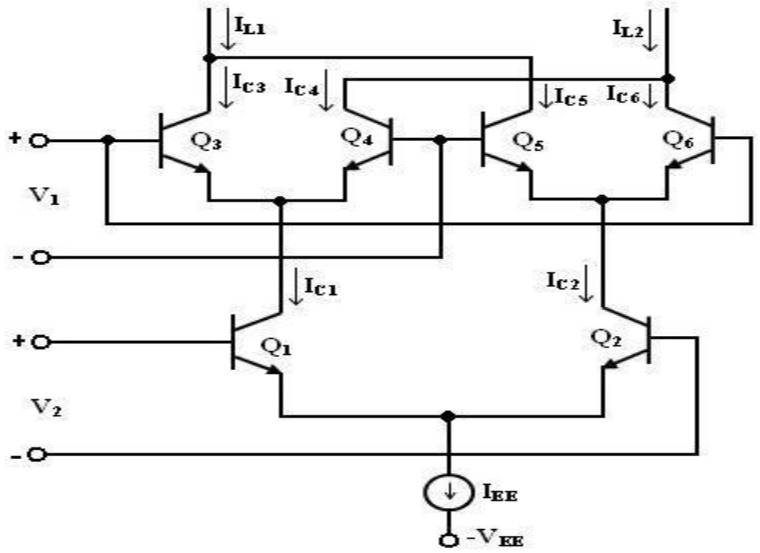


Fig. 3.8 Gilbert multiplier cell

The collector current ofQ_3 and Q_4 are given by

$$I_{c3}= \frac{I_{C1}}{1+e^{-v1/vT}} \text{ and } I_{c4}= \frac{I_{C1}}{1+e^{v1/vT}}$$

Similarly, the collector current ofQ_5 and Q_6 are given by

$$I_{c5}= \frac{I_{C2}}{1+e^{-v1/vT}} \text{ and } I_{c6}= \frac{I_{C2}}{1+e^{v1/vT}}$$

Collector current I_{C1} and I_{c2} of transistors Q1 and Q2 can be expressed as

$$I_{c1}= \frac{I_{EE}}{1+e^{-v1/vT}} \text{ and } I_{c2}= \frac{I_{EE}}{1+e^{v1/vT}}$$

Substituting above equation I_{C4} and I_{c5}

$$I_{c3}= \frac{I_{EE}}{[1+e^{-v2/vT}]+[1+e^{v1/vT}]} \text{ and } I_{c4}= \frac{I_{EE}}{[1+e^{-v2/vT}]+[1+e^{v1/vT}]}$$

Similarly substituting I_{c2} in I_{c5} and I_{c6} we get

$$I_{c5}= \frac{I_{EE}}{[1+e^{v2/vT}]+[1+e^{v1/vT}]} \text{ and } I_{c6}= \frac{I_{EE}}{[1+e^{v2/vT}]+[1+e^{v1/vT}]}$$

The differential output currentΔI is given by

$\Delta I = I_{L1} - I_{L2}$

$=(I_{C3}+I_{C5})-(I_{C4}+I_{C6})$

$=(I_{C3} - I_{C6})-(I_{C4} - I_{C5})$

I=I EE tanh(V1/2VT) tanh(V2/2VT)

3.3 Variable Transconductance Technique:

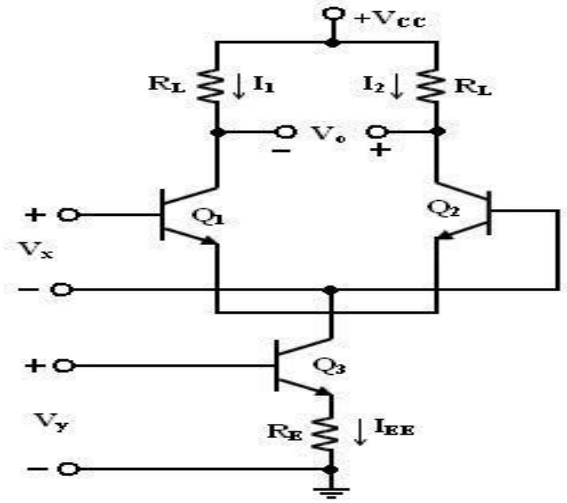


Fig. 3.9 Differential stage of the Tran conductance multiplier

The variable transconductance technique makes use of the dependence characteristic of the transistor transconductance parameter on the emitter current bias applied. A simple differential circuit arrangement depicting the principle is shown in figure.

- The relationship between V0 and Vx .is given by V0 = gm RL VX where gm = IEE /VT is thetransconductance of the stage.
- Application of a second input Vy to the reference current source of the differential amplifier can vary gm.
- Thus, if RE IEE >>VBE, the bias voltage Vy is related to IEE by the relation Vy = IEE RE.
- Then, the overall voltage transfer expression is given by

$$V0 = gm\ RLVx = (Vy/VTRE)VxRL$$

3.4 Analog Multiplier ICs

Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages.

Important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation.

These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements. The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.

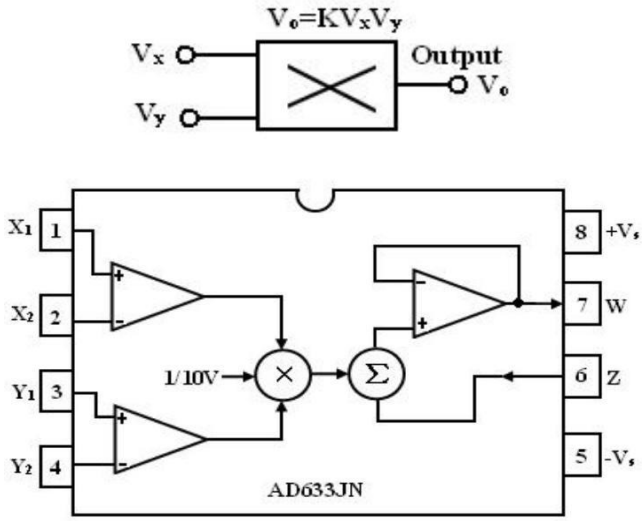


Fig. 3.10 Multiplier IC and its symbol

- The AD633 multiplier is a four – quadrant analog multiplier.
- It possesses high input impedance; this characteristic makes the loading effect on the signal source negligible.
- It can operate with supply voltages ranging from ±18V. TheIC does not require external components.
- The typical range of the two input signals is ±10V.

The schematic representation of an analog multiplier is shown in figure. The output V0 is the product of the two inputs Vx and Vy is divided by a reference voltage Vref. Normally, the reference voltage Vref is internally set to 10V. Therefore, V0 =VxVy/10. In other words, the basic input – output relationship can be defined by KVxVy when K = 1/10, a constant. Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V. Thus, it can be noted that, as long as Vx< 10V and Vy< 10V, the multiplier output will not saturate.

Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier are shown in figure. Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

Applications of Multiplier ICs:

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doublers
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

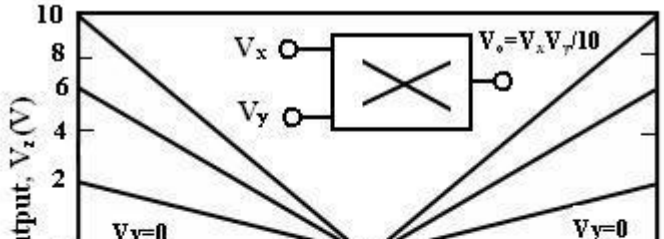


Fig.3.11 Transfer characteristics of a typical four-quadrant multiplier

Voltage Squarer:

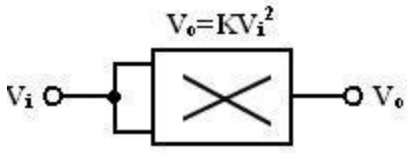


Fig. 3.12 voltage squarer circuit

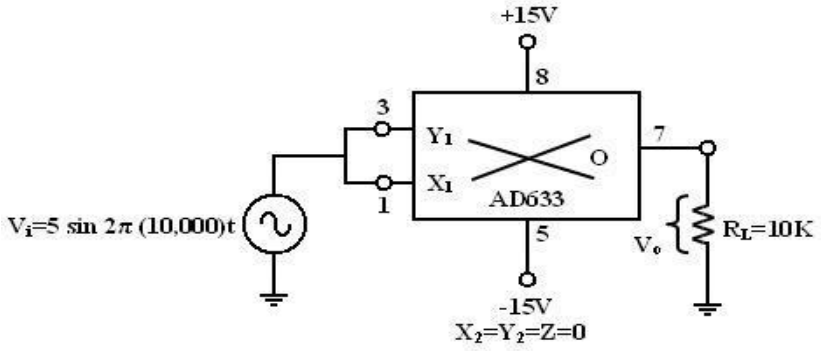
Figure shows the multiplier IC connected as a squaring circuit. The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10V. The input voltage Vi to be squared is simply connected to both the input terminals, and hence we have, Vx = Vy = Vi and the output is V0 = KVi2. The circuit thus performs the squaring operation. This application can be extended for frequency doubling applications.

Frequency doublers:

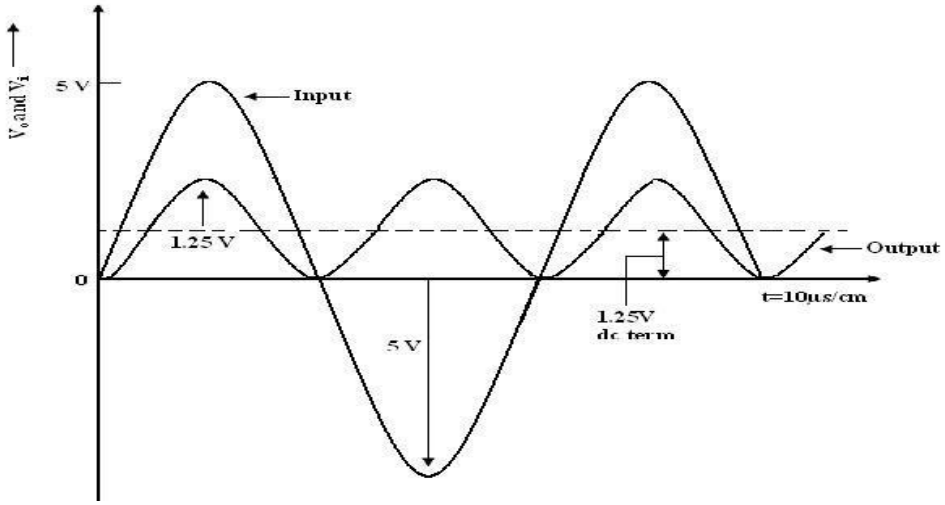
Figure shows the squaring circuit connected for frequency doubling operation. A sine-wave signal Vi has a peak amplitude of Av and frequency of f Hz. Then, the output voltage of the doublers

$V_O=\frac{Avsin2\pi ft*Avsin2\pi ft}{10}=\frac{Av^2sin2\pi ft}{10}=\frac{Av^2}{20}$(1-4cos 4πft)

Assuming a peak amplitude Av of 5V and frequency f of 10KHz, V0 =1.25–1.25 cos2 20000) t. The first term represents the dc term of 1.25V peak amplitude. The input and output waveforms are shown in figure. The output waveforms ripple with twice the input frequency in the rectified output of the input signal. This forms the principle of application of analog multiplier as rectifier of ac signals.



(a)



(b)

Fig. 3.13 (a) circuit diagram and (b) input –output waveform of frequency doubler

The dc component of output V0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

Voltage Divider:

In voltage divider circuit the division is achieved by connecting the multiplier in the feedback loop of an op-amp.

The voltages Vden and Vnum represent the two input voltages, Vdm forms one input of the multiplier, and output of op-amp VoA forms the second input.

The output VOA forms the second input. The output VOM of the multiplier is connected back of op- amp in the feedback loop. Then the characteristic operation of the multiplier gives

Vom = KVOA Vdm (1)

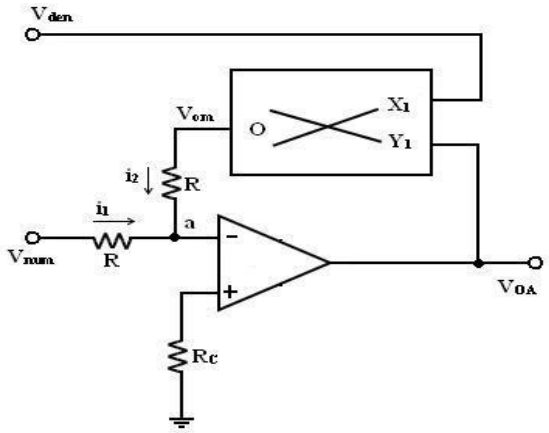


Fig 3.14 divider circuit

As shown in figure, no input signal current can flow into the inverting input terminal of op-amp, which is at virtual ground. Therefore, at the junction a, i1 +i2 =0, the current i1 = Vnum / R, where R is the input resistance and the current i2 = Vom /R. With virtual ground existing at a,

$$i1+i2 = \text{Vnum} / R + \text{Vom} /R = 0$$

$$KV\ OA\ V\ den = -\ V\ num \quad or$$

$$voA = -\ vnum/Kvden$$

where*Vnum* and *Vden* are the numerator and denominator voltages respectively. Therefore, the voltage division operation is achieved. *Vnum* can be a positive or negative voltage and *Vden* can have only positive values to ensure negative feedback. When *Vdm* is changed, the gain 10/*Vdm* changes, and this feature is used in automatic gain control (AGC) circuits.

- **Square Rooter:**

The divider voltage can be used to find the square root of a signal by connecting both inputs of the multiplier to the output of the op-amp. *Substituting* equal in magnitude but opposite in polarity (with respect to ground) to Vi. But we know that Vom is one- term (Scale factor) of V0 * V0 or -Vi = Vom = $V^2/1$ 0

Solving for V0 and eliminating √-1 yields. V0 = √10|Vi |

Eqn. states that V0 equals the square root of 10 times the absolute magnitude of Vi.

The input voltage Vi must be negative, or else, the op-amp saturates.

The range of Vi is between -1 and -10V. Voltages less than -1V will cause inaccuracies in the result.

The diode prevents negative saturation for positive polarity Vi signals. For positive values of Vi the diode connections are reversed.

- **Phase Angle detector:**

The multiplier configured for phase angle detection measurement is shown in figure. When two sine-waves of the same frequency are applied to the inputs of the multiplier, the output V0 has a dc component and an AC component.

The trigonometric identity shows that Sin A sin B =1/2 (cos (A-B) – cos (A+B)).

When the two frequencies are equal, but with different phase angles, e.g. A=2πft+θ for signal Vx and B= 2πft for signal Vy, then using the identity

sin (2 *ft*+)][sin2 *ft*)]=1/2[cos -cos(4 *ft* +)]=1/2(dc- the double frequency term) Therefore, when the two input signals VxandVyare applied to the multiplier,

V0 (dc) is given by

$$v_v(dc) = \frac{v_{xp}v_{yp}}{20}\cos\theta$$

where*Vxp* and *Vyp* are the peak voltage amplitudes of the signals Vx and Vy. Thus, the output V0(dc) depends on the factor cos θ. A dc voltmeter can be calibrated as a phase angle meter when the product of Vxp and Vyp is made equal to 20. Then, a (0-1) V range dc voltmeter can directly read cos θ, with the meter calibrated directly in degrees from a cosine table. The input and output waveforms are shown in figure.

Then the above eqn becomes V0 (dc) = cos θ, if we make the product VxpVyp = 20 or in other words, Vxp – Vyp = 4.47V.

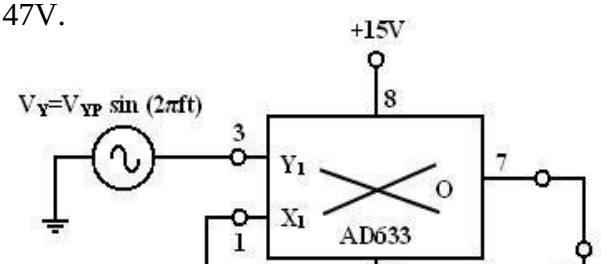


Fig 3.15 Phase angle measurement circuit diagram

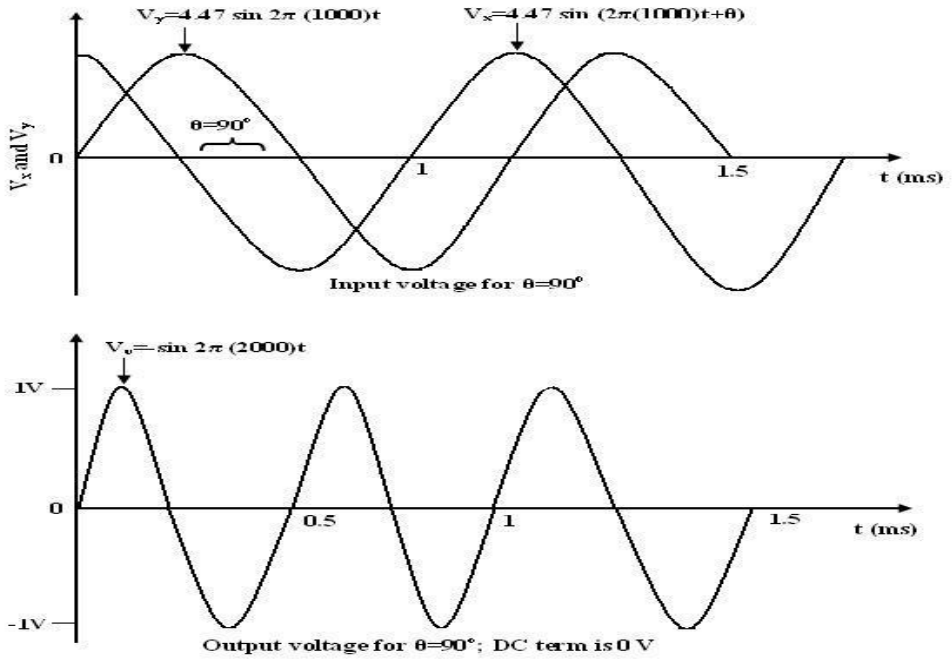


Fig. 3.16 input- output waveforms of phase angle detector

3.5 Operation of Basic Phase Locked Loop

The PLL consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency fIN with feedback frequency fOUT.

The output of the phase detector is proportional to the phase difference between fIN&fOUT. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage

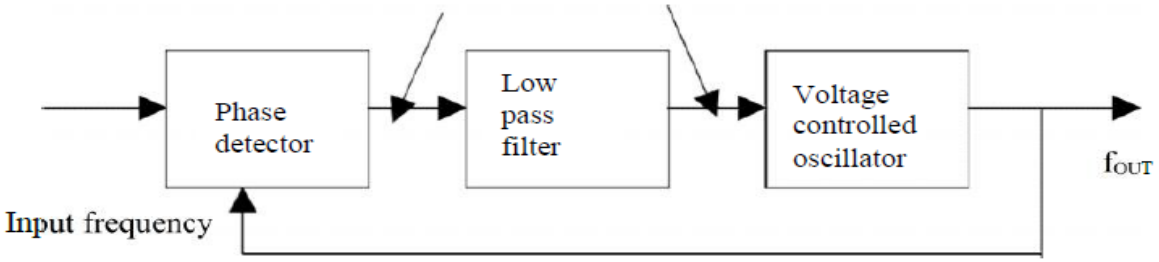


Fig 3.17 Block diagram of PLL

- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.

Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode. When Phase locked, the loop tracks any change in the input frequency through its repetitive action.

If an input signal vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output vo of the VCO. If the two signals differ in frequency of the incoming signal to that of the output vo of the VCO.

The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs - fo) components at its output.

The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO.

The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference φ. This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an inputsignal is called the capture range. This parameter is also expressed as percentage of fo.

Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. Thisdepends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

3.5.1 Phase Detector

Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies. Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively. Even though most monolithic PLL integrated circuits use analog phase detectors.

Ex for Analog: Double-balanced mixer

Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

- Ex-OR Phase Detector:

This uses an exclusive OR gate. The output of the Ex-OR gate is high only when fIN or fOUT is high.

The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs. The maximum dc output voltage occurs when the phase difference is Π radians or 180 degrees. The slope of the curve between 0 or Π radians is the conversion gain kp of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc= 5V, the conversion gain Kp is

$$k_{p=}\frac{5}{\pi}=1.59\,rad$$

Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.

RS FF is triggered, i.e., the output of the detector changes its logic state on the positive edge of the inputs fIN&fOUT

- Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- Phase detector 2, if quadrature lock is desired, when detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.

3.5.2 Low – Pass filter

The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise. LPF controls the characteristics of the phase locked loop. i.e., capture range, lock ranges, bandwidth

- Lock range(Tracking range):
  The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.
- Capture range:
  Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.
- Filter Bandwidth:
  Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

3.5.4 Voltage Controlled Oscillator (VCO):

The third section of PLL is the VCO; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz.

3.5.5 Feedback path and optional divider:

Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer. A programmable divider is particularly useful in radio Transmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

Some PLLs also include a divider between the reference clock and the reference input to the phase detector. If this divider divides by *M*, it allows the VCO to multiply the reference frequency by *N* / *M*. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful.

Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal.

The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows. Let the input to the phase detector be *xc*(*t*) and the output of the voltage- controlled oscillator (VCO) is *xr*(*t*) with frequency ω*r*(*t*), then the output of the phase detector *xm*(*t*) is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input *y*(*t*) as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where*gv* is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0 \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

where

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$$xf(t) = F\text{filter}(xm(t))$$

where Filter is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$$y(t) = xf(t) = F\text{filter}(xm(t))$$

We can deduce how the PLL reacts to a sinusoidal input signal:

$$xc(t) = Ac\sin(\omega ct).$$

The output of the phase detector then is:

$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model Of the phase-locked loop. If we can make $\omega_f = \omega_c$then the sin (.)can be approximated by its argument resulting in:

$$y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$$

The phase-locked loop is said to be locked if this is the case.

3.6 Control System Analysis/ Closed Loop Analysis Of PLL

Phase locked loops can also be analyzed as control systems by applying the Laplace transform. The loop response can be written as:

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where

- θo is the output phase in radians
- θi is the input phase in radians
- *Kp*is the phase detector gain in volts per radian
- *Kv*is the VCO gain in radians per volt-second
- *F*(*s*) is the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

This is the form of a classic harmonic oscillator. The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where

- ζ is the damping factor
- ωn is the natural frequency of the loop.

for one pole model $\omega_n = \sqrt{\frac{K_p K_v}{RC}} \qquad \varsigma = \frac{1}{2\sqrt{K_p K_v RC}}$

The loop natural frequency is a measure of the response time of the loop, and the damping factor is a measure of the overshoot and ringing. Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping). With a single pole filter, it is not possible to control the loop frequency and damping factor independently. For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$
$$\omega_c = K_p K_v \sqrt{2}$$

A slightly more effective filter, the lag-lead filter includes one pole and one zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

This filter has two time constants

$$\tau 1 = C(R1 + R2)\ \tau 2$$

$$= CR2$$

Substituting above yields the following natural frequency and damping factor

$$\omega_n - \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

Real world loop filter design can be much more complex eg using higher order filters to reduce various types or source of phase noise.

Applications of PLL:

The PLL principle has been used in applications such as

FM stereo decoders

- motor speed control
- tracking filters
- FM modulation and demodulation
- FSK modulation
- Frequency multiplier
- Frequency synthesis etc.,

Example PLL ICs:560 series (560, 561, 562, 564, 565 & 567)

3.7 Voltage Controlled Oscillator:

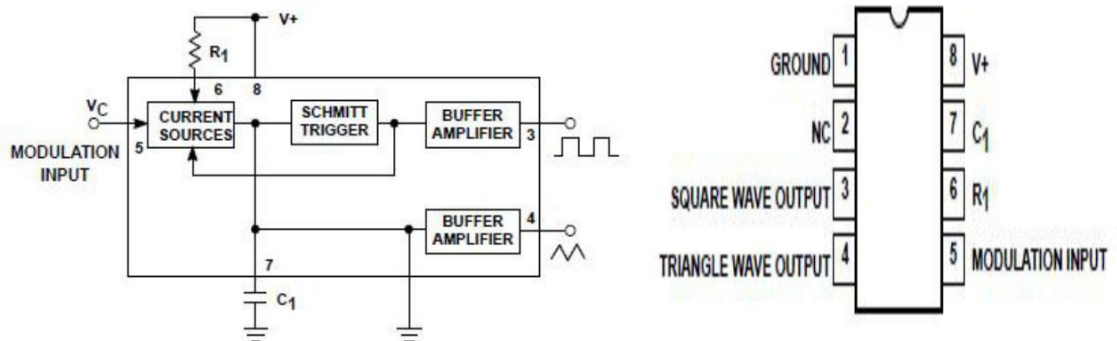


Fig. 3.18 Pin diagram and block diagram of VCO

Referring to the circuit in the above figure, the capacitor c1 is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage vc applied at the modulating input (pin 5) or by changing the timing resistor R1 external to the IC chip. The voltage at pin 6 is held at the same voltage as pin 5.

Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R1 and thereby decreasing the charging current.

The voltage across the capacitor C1 is applied to the inverting input terminal of Schmitt trigger via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to Vcc and 1.5 Vcc. If Ra = Rb in the positive feedback loop, the voltage at the non-inverting input terminal of Schmitt trigger swings from 0.5 Vcc to 0.25 Vcc.

When the voltage on the capacitor c1 exceeds 0.5 Vcc during charging, the output of the Schmitt trigger goes LOW (0.5 Vcc). The capacitor now discharges and when it is at 0.25 Vcc, the output of Schmitt trigger goes HIGH (Vcc). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across c1 which is also available at pin 4.

The square wave output of the Schmitt trigger is inverted by buffer amplifier at pin 3. The output waveforms are shown near the pins 4 and 3.

The output frequency of the VCO can be given as follows:

$$f_o = \frac{2\,[(V+) - (V_C)]}{R_1\, C_1\, V+}$$

where V+ is Vcc.

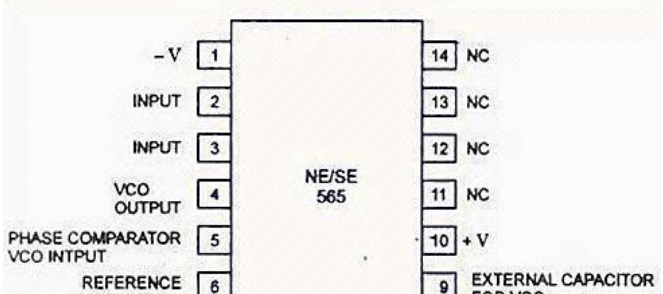
The output frequency of the VCO can be changed either by (i) R1, (ii) c1 or (iii) the voltage vc at the modulating input terminal pin 5. The voltage vc can be varied by connecting a R1R2 circuit as shown in the figure below. The components R1and c1 are first selected so that VCO output frequency lies in the centre of the operating frequency range.

Now the modulating input voltage is usually varied from 0.75 Vcc to Vcc which can produce a frequency variation of about 10 to 1.

The signetics NE/SE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565 & 567 differ mainly in operating frequency range, poser supply requirements & frequency& bandwidth adjustment ranges.

3.8 Monolithic Phase Locked Loops (PLL IC 565):

Pin Configuration of PLL IC 565



Basic Block Diagram Representation of IC 565

The important electrical characteristics of the 565 PLL are,

- Operating frequency range: 0.001Hz to 500 Khz.
- Operating voltage range: ±6 to ±12v
- Input level required for tracking: 10mv rms min to 3 Vpp max
- Input impedance: 10 K ohms typically.
- Output sink current: 1mA
- Output source current: 10 mA

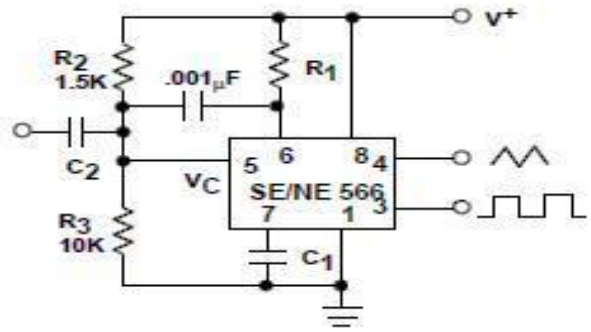
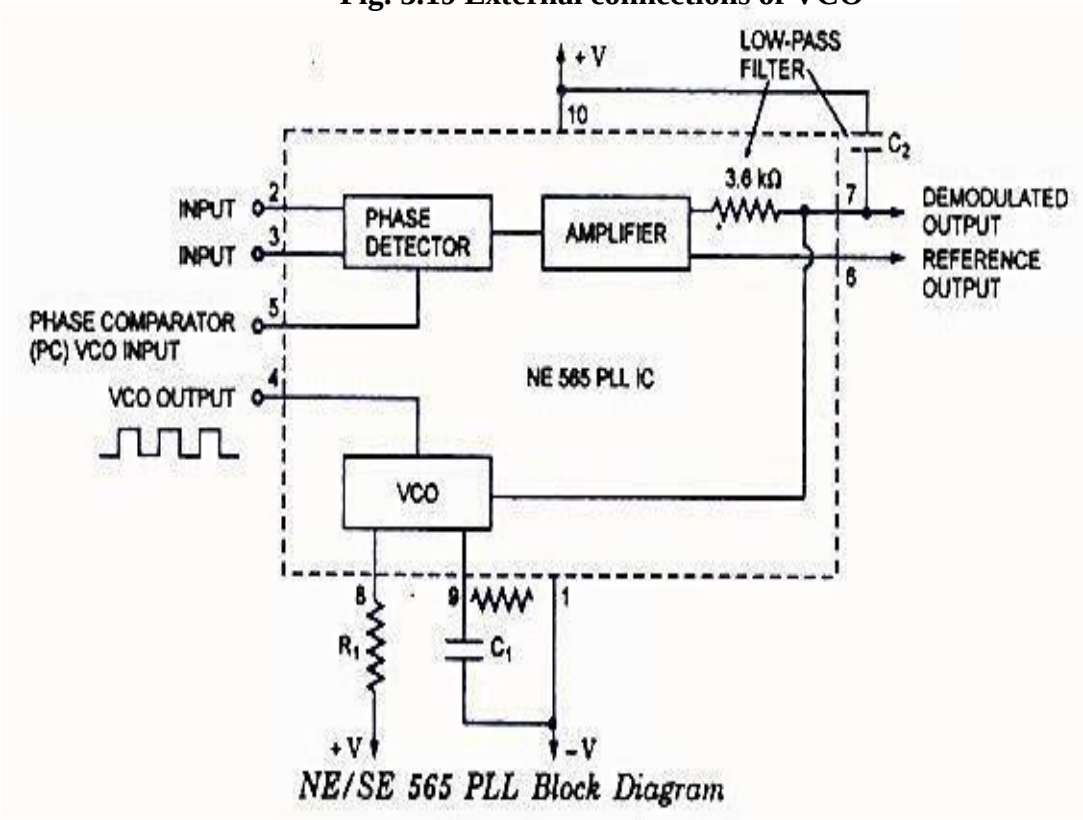


Fig. 3.19 External connections of VCO



NE/SE 565 PLL Block Diagram

The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by

fOUT = 1.2/ 4*R*1*C*1

where R1&C1 are an external resistor & a capacitor connected to pins 8 & 9.

- The VCO free-running frequency fOUT is adjusted externally with R1 & C1 to be at the center of the input frequency range.
- C1 can be any value; R1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C2 connected between 7 & +V.
- The filter capacitor C2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.

The lock range fL& capture range fc of PLL is given by,

$$\Delta fL = \pm 7.8 \, fout / VHz$$

Where f= free running frequency of VCO (Hz)

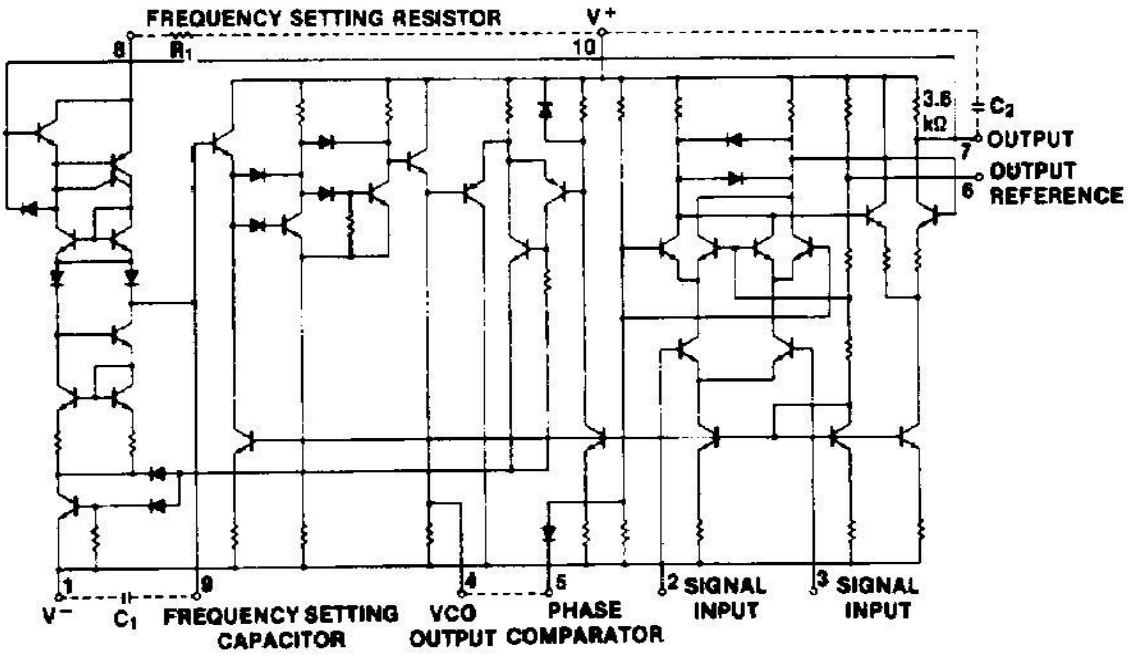
V=+Vcc-(-Vcc) volts

$$\Delta f_C = \pm [\, \Delta fL/(2\Pi)(3.6)(10^3)C2 \,]^{1/2}$$

5.9 Monolithic PLL IC 565 applications:

The output from a PLL system can be obtained either as the voltage signal vc(t) corresponding to the error voltage in the feedback loop, or as a frequency signal at VCO output terminal. Thevoltage output is used in frequency discriminator applications whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications

The circuit diagram of LM565 PLL



When PLL is locked to an input frequency, the error voltage vc(t) is proportional to (fs-fo). If the input frequency is varied as in the case of FM signal vc will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed below.

- **Frequency Multiplier:**

Frequency divider is inserted between the VCO & phase comparator. Since the output of the divider is locked to the fIN, VCO is actually running at a multiple of the input frequency.

The desired amount of multiplication can be obtained by selecting a proper divide-by-N network, where N is an integer.

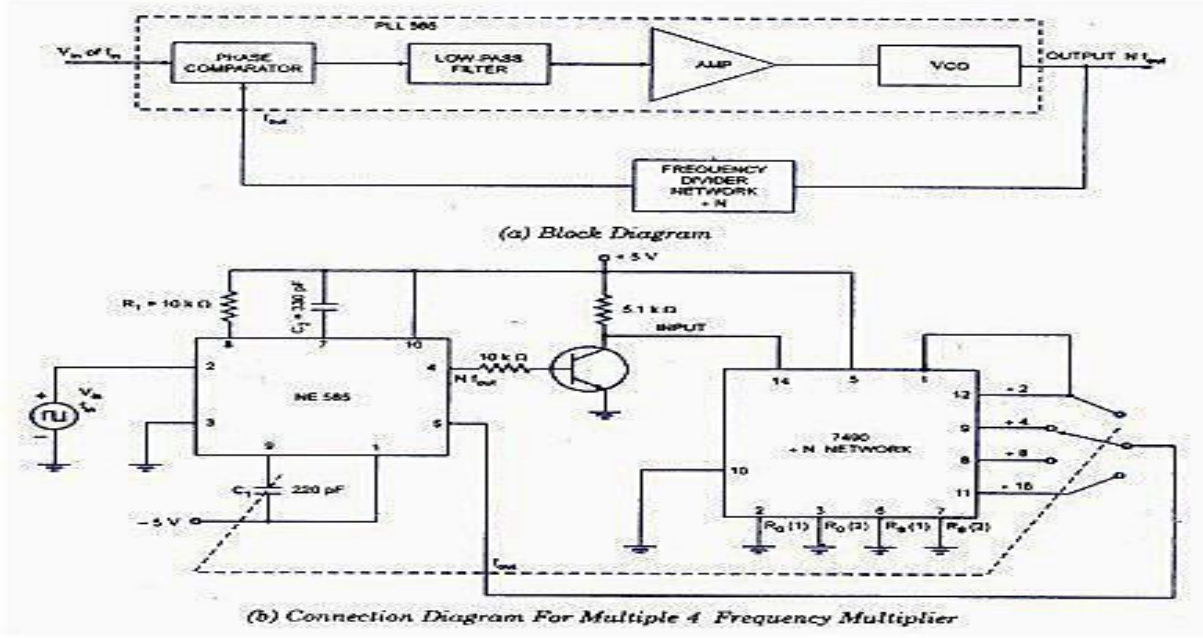
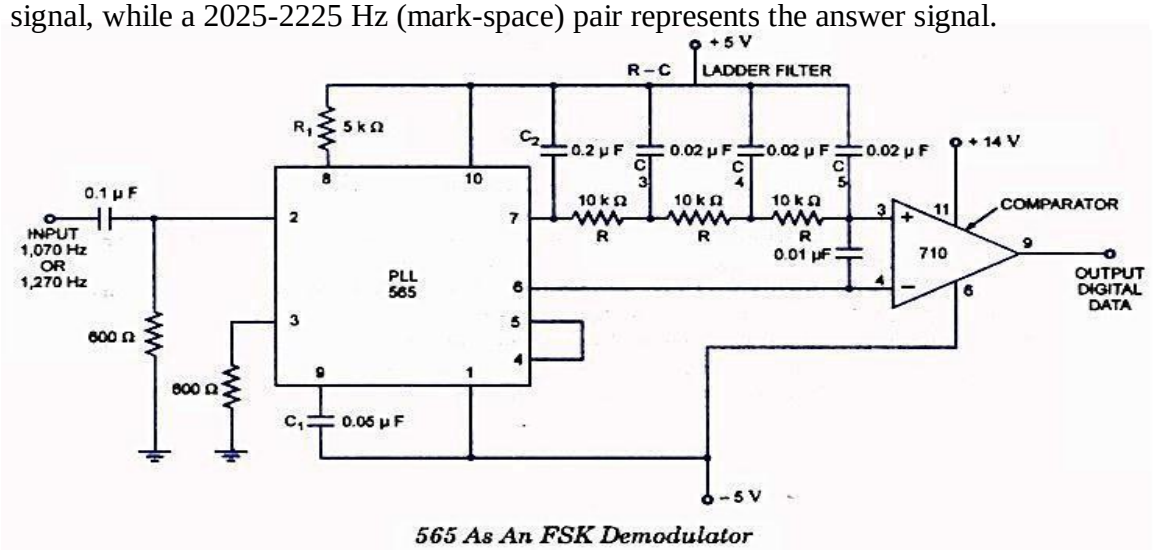


Fig. 3.20 Frequency multiplier using PLL

- **Frequency Shift Keying (FSK) demodulator:**

In computer peripheral & radio (wireless) communication the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a FSK. The frequency corresponding to logic 1 & logic 0 states are commonly called the mark & space frequency.

For example, When transmitting teletype writer information using a modulator-demodulator (modem) a 1070-1270 (mark-space) pair represents the originate signal, while a 2025-2225 Hz (mark-space) pair represents the answer signal.



565 As An FSK Demodulator

FSK Generator:

- The FSK generator is formed by using a 555 as an astablemultivibrator, whose frequency is controlled by the state of transistor Q1.
- In other words, the output frequency of the FSK generator depends on the logic state of the digital data input.
- 150 Hz is one the standards frequencies at which the data are commonly transmitted.
- When the input is logic 1, the transistor Q1 is off. Under the condition, 555 timer works in its normal mode as an astablemultivibrator i.e., capacitor C charges through RA & RB to 2/3Vcc & discharges through RB to 1/3 Vcc. Thus capacitor C charges & discharges between 2/3 Vcc& 1/3 Vcc as long as the input is logic 1.
- The frequency of the output waveformis given
  - $$fo = \frac{1.45}{(RA+2RB)C} = 1070\ HZ(mark\ frequency)$$
- When the input is logic 0, (Q1 is ON saturated) which in turn connects the resistance Rc across RA. This action reduces the charging time of capacitor C1 increases the output frequency,which is given by

$$fo = \frac{1.45}{(RA||RC + 2RB)C} = 1270\ HZ(mark\ frequency)$$

By proper selection of resistance Rc, this frequency is adjusted to equal the space frequency of 1270 Hz. The difference between the FSK signals of 1070 Hz & 1270 Hz is 200 Hz, this difference is called “frequency shift”.

- The output 150 Hz can be made by connecting a voltage comparator between the output of the ladder filter and pin 6 of PLL.

- The VCO frequency is adjusted with R1 so that at fIN = 1070 Hz.

FSK Demodulator:

- The output of 555 FSK generators is applied to the 565 FSK demodulator.
- Capacitive coupling is used at the input to remove dc line.
- At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- R1 & C1 determine the free running frequency of the VCO, 3 stages RC ladder filter is used to remove the carrier component from the output.

Applications:

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator. The figure below shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

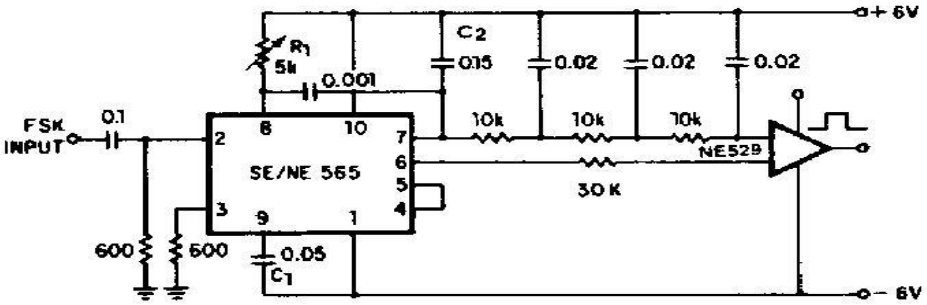


Fig. 3.21 FSK demodulator circuit

- **AM Demodulation:**

A PLL may be used to demodulate AM signals as shown in the figure below. The PLL is locked to the carrier frequency of the incoming AM signal. The output of VCO which has the same frequency as the carrier, butunmodulated is fed to the multiplier. Since VCO output is always 90^0before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

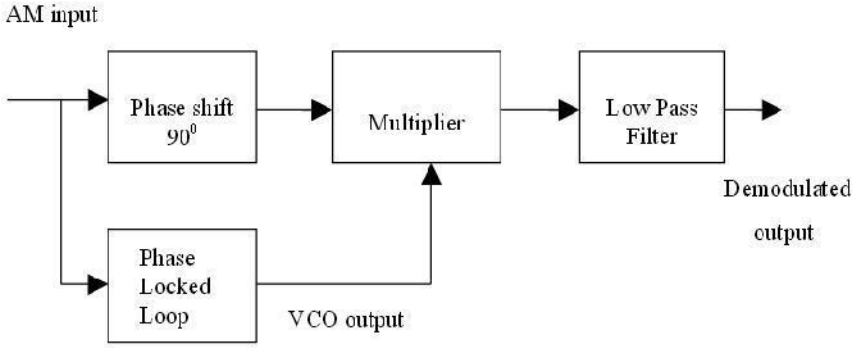


Fig.3.22 AM demodulator

- **FM Demodulation:**

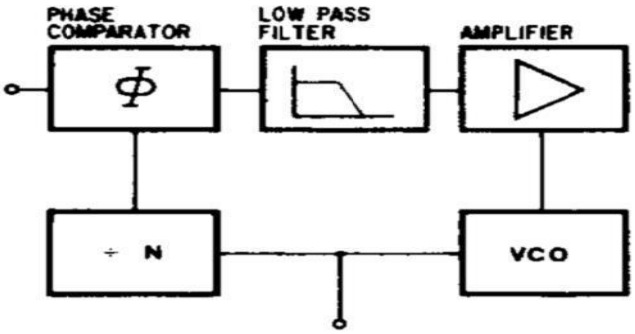
If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.

The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

- **Frequency multiplication/division:**

The block diagram shown below shows a frequency multiplier/divider using PLL. A divide by N network is inserter between the VCO output and the phase comparator input. In the locked state, the VCO output frequency fo is given by fo = Nfs. The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.



The circuit of the figure above can also be used for frequency division. Since the VCOoutput (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal fs. The output fo of VCO is now given by fo=fs/m

- PLL Frequency Synthesis:

In digital wireless communication systems (GSM, CDMA etc), PLL's are used to provide the Local Oscillator (LO) for up-conversion during transmission, and down-conversion during reception. In most cellular handsets this function has been largely integrated into a single integrated circuit to reduce the cost and size of the handset.

However due to the high performance required of base station terminals, the transmission and reception circuits are built with discrete components to achieve the levels of performance

required. GSM LO modules are typically built with a Frequency Synthesizer integrated circuit, and discrete resonator VCO's.

Principle of PLL synthesizers

A phase locked loop does for frequency what the Automatic Gain Control does for voltage. It compares the frequencies of two signals and produces an error signal which is proportional to the difference between the input frequencies.

The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency. The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop.

If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error. Thus the output is *locked* to the frequency at the other input. This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency.

The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.

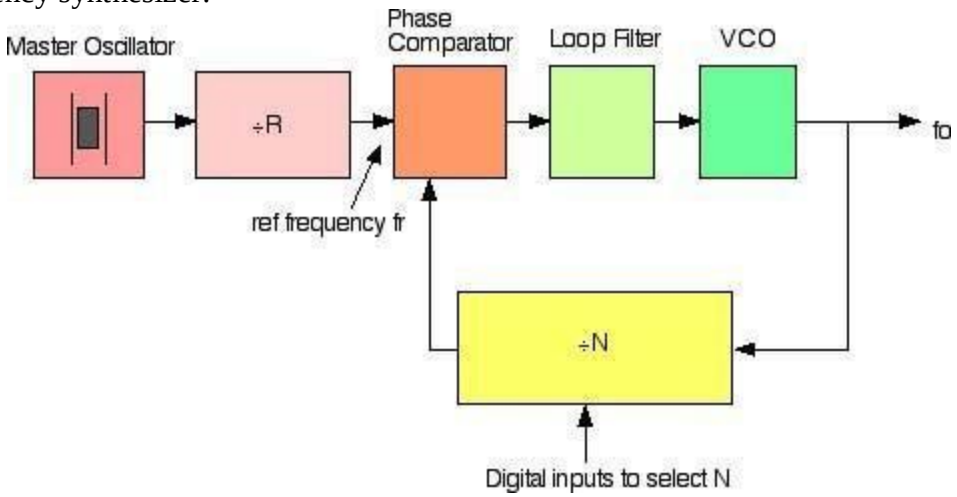


Fig. 2.24 PLL based frequency synthesizer

The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the feedback input. This is usually in the form of a digital counter, with the output signal acting as a clock signal.

The counter is preset to some initial count value, and counts down at each cycle of the clock signal. When it reaches zero, the counter output changes state and the count value is reloaded.

This circuit is straightforward to implement using flip-flops, and because it is digital in nature, is very easy to interface to other digital components or a microprocessor. This allows the frequency output by the synthesizer to be easily controlled by a digital system.

Example:

Suppose the reference signal is 100 kHz, and the divider can be preset to any value between 1 and.The error signal produced by the comparator will only be zero when the output of the

divider is also 100 kHz. For this to be the case, the VCO must run at a frequency which is 100 kHz x the divider count value.

Thus it will produce an output of 100 kHz for a count of 1, 200 kHz for a count of 2, 1 MHz for a count of 10 and so on. Note that only whole multiples of the reference frequency can be obtained with the simplest integer N dividers. Fractional N dividers are readily available

Practical considerations:

In practice this type of frequency synthesizer cannot operate over a very wide range of frequencies, because the comparator will have a limited bandwidth and may suffer from aliasing problems. This would lead to false locking situations, or an inability to lock at all. In addition, it is hard to make a high frequency VCO that operates over a very wide range.

This is due to several factors, but the primary restriction is the limited capacitance range of varactor diodes. However, in most systems where a synthesizer is used, we are not after a huge range, but rather a finite number over some defined range, such as a number of radio channels in a specific band.

Many radio applications require frequencies that are higher than can be directly input to the digital counter. To overcome this, the entire counter could be constructed using high-speed logic such as ECL, or more commonly, using a fast initial division stage called a *prescaler* which reduces the frequency to a manageable level.

Since the prescaler is part of the overall division ratio, a fixed prescaler can cause problems designing a system with narrow channel spacing's - typically encountered in radio applications. This can be overcome using a dual-modulus prescaler.

Further practical aspects concern the amount of time the system can switch from channel to channel, time to lock when first switched on, and how much noise there is in the output. All of these are a function of the *loop filter* of the system, which is a low-pass filter placed between the output of the frequency comparator and the input of the VCO.

Usually the output of a frequency comparator is in the form of short error pulses, but the input of the VCO must be a smooth noise- free DC voltage. (Any noise on this signal naturally causes frequency modulation of the VCO).

Heavy filtering will make the VCO slow to respond to changes, causing drift and slow response time, but light filtering will produce noise and other problems with harmonics. Thus the design of the filter is critical to the performance of the system and in fact the main area that a designer will concentrate on when building a synthesizer system.

UNIT IV
ANALOG TO DIGITAL & DIGITAL TO ANALOG CONVERTERS

4. 1 1Analog to Digital Conversion

The natural state of audio and video signals is analog. When digital technology was not yet around, they are recorded or played back in analog devices like vinyl discs and cassette tapes. The storage capacity of these devices is limited and doing multiple runs of re-recording and editing produced poor signal quality. Developments in digital technology like the CD, DVD, Blu-ray, flash devices and other memory devices addressed these problems. For these devices to be used, the analog signals are first converted to digital signals using analog to digital conversion (ADC)**.** For the recorded audio and video signals to be heard and viewed again, the reverse process of digital to analog conversion (DAC) is used.

ADC and DAC are also used in interfacing digital circuits to analog systems. Typical applications are control and monitoring of temperature, water level, pressure and other real-world data.

An ADC inputs an analog signal such as voltage or current and outputs a digital signal in the form of a binary number. A DAC, on the other hand, inputs the binary number and outputs the corresponding analog voltage or current signal.

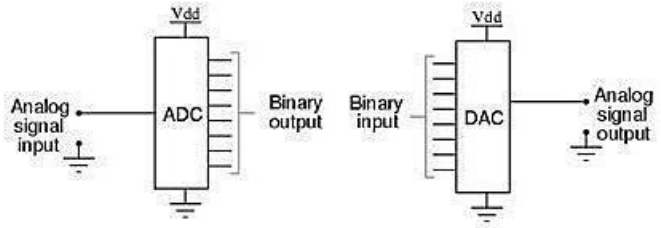


Fig 4.1 ADC and DAC circuits

Sampling rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the *sampling rate* or *sampling frequency* of the converter.

A continuously varying band limited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be *exactly* reproduced from the discrete-time values by an interpolation formula. The accuracy is

limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the *conversion time*). An input *c*ircuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity is intrinsic to any analog-to-digital conversion. There is also a so called *aperture error* which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value).

These errors are measured in a unit called the *LSB*, which is an abbreviation for least significant bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

Quantization error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.

In the general case, the original signal is much larger than one LSB. When this happens, the quantization error is not correlated with the signal, and has a uniform distribution. Its RMS value is the standard deviation of this distribution, given by $\frac{1}{\sqrt{12}}\text{LSB} \approx 0.289\,\text{LSB}$

In the eight-bit ADC example, this represents 0.113% of the full signal range.

At lower levels the quantizing error becomes dependent of the input signal, resulting in distortion. This distortion is created after the anti-aliasing filter, and if these distortions are above 1/2 the sample rate they will alias back into the audio band. In order to make the Quantizing error independent of the input signal, noise with amplitude of 1 quantization step is added to the signal. This slightly reduces signal to noise ratio, but completely eliminates the distortion. It is known as dither.

Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, resulting in their output to deviate from a linear function (or some other function, in the case of a deliberately nonlinear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

Important parameters for linearity are integral non-linearity (INL) and differential non-linearity (DNL). These non-linear ties reduce the dynamic range of the signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

DAC- Specifications

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = VoFS / (2 n - 1) = 1 LSB increment Where 'n' is the number of input bits 'VoFS' is the full scale output voltage.

Example:

Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

Table 4.1 Resolution for DAC

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem. Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have beenremoved. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage.Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absoluteaccuracy.

Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/Aconverters are having a linearity error as low as 0.001% of full scale. The linearity of a D/Aconverter is defined as the precision or exactness with which the digital input is converted intoanalog output. An ideal D/A converter produces equal increments or step sizes at output for everychange in equal increments of binary input.

Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristic is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition. When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

4.2 Digital to Analog Conversion

A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure). In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal. A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses.

Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulse density modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal. By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital Sampling introduces quantization that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error.

DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

4.3 Specifications:

Resolution: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (21) levels while an 8 bit DAC is designed for 256 (28) levels. Resolution is related to the

Effective number of bits (ENOB) which is a measurement of the actual resolution attained by the DAC.

Maximum sampling frequency: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard

samples audio at kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other sample rates only through (often poor) internal resampling.

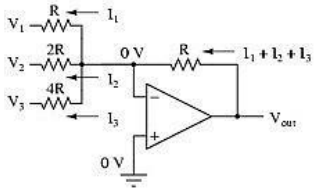
Monotonicity: This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

THD+N: This is a measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

Dynamic range: This is a measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to DAC resolution and noise floor. Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

4.4 Binary-Weighted Resistor DAC

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).



$$V_{out} = -(V_1 + \frac{V_2}{2} + \frac{V_3}{4})$$

Fig. 4.2 Binary weighted DAC

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:

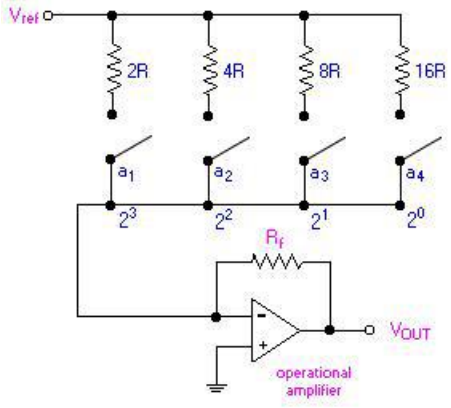


Fig. 4.3 weighted resistor DAC using Op-amp

The binary inputs, a_i (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch. The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, Vref.

For a 4-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -iR_f$$
$$= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right)$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)$$

The negative sign associated with the analog output is due to the connection to aSumming amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa). For an n-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref}R_f}{R}\sum_{i=1}^{n}\frac{a_i}{2^i}$$

The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

1.The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k Ω, then the LSB is a staggering 2 MΩ.

2. The maintenance of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintains an accurate ratio especially with variations in temperature.

4.5 R-2R Ladder DAC

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages. A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit.

The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).

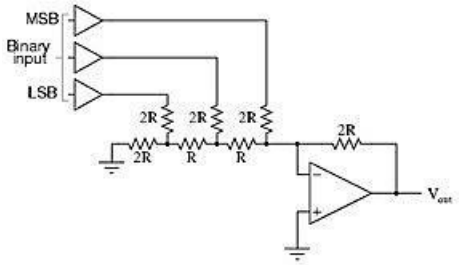


Fig.4.4 Ladder type DAC circuit

Vout = - (VMSB + Vn + VLSB) = - (VRef + VRef/2 + VRef/ 4)

Table 4.2 operation of an R-2R ladder DAC

| Binary | Output voltage |

000	0.00 V
001	-1.25 V
010	-2.50 V
011	-3.75 V
100	-5.00 V
101	-6.25 V
110	-7.50 V
111	-8.75 V

4.6 Inverted or Current Mode DAC

Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into *i*1,*i*2, *i*3 ……*i*n. in each arm. The currents are either diverted to the ground bus (*io*) or to the Virtual-ground bus *(io)*.

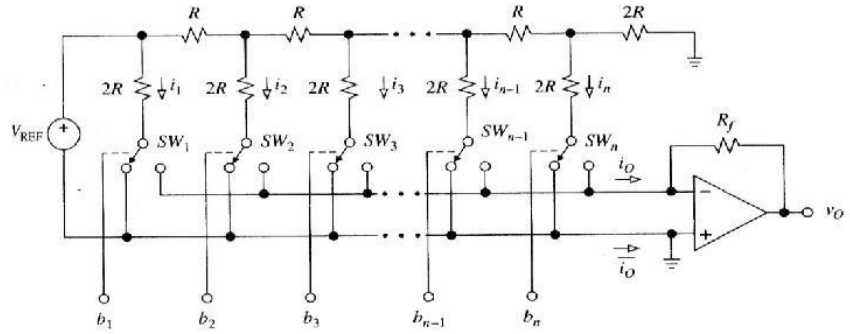


Fig.4.5 Current mode DAC

The currents are given as

*i*1 = VREF/2R = (VREF/R) 2^{-1}, *i*2 = (VREF)/2)/2R = (VREF/R) 2^{-2}……*in* = (VREF/R) 2^{-n}.

And the relationship between the currents are given as

i2 = i1/2, i3 = i1/4, i4 = i1/8, in = i1/ 2^{n-1}

Using the bits to identify the status of the switches, and letting V0 = -R*io*gives

V0 = - (Rf/R) VREF (b1 2^{-1} + b2 2^{-2}+ …….. + bn 2^{-n})

The two currents *io*and *io*are complementary to each other and the potential of *io*bus must be sufficiently close to that of the *io*bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

Advantages

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

Voltage Mode DAC

This is the alternative mode of DAC and is called so because the 2R resistance in the shunt path is switched between two voltages named as VL and VH. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1). The voltage of this node changes in steps of 2^{-n} (VH - VL) from

the minimum voltage of Vo = VL to the maximum of Vo = VH – 2^{-n} (VH - VL).

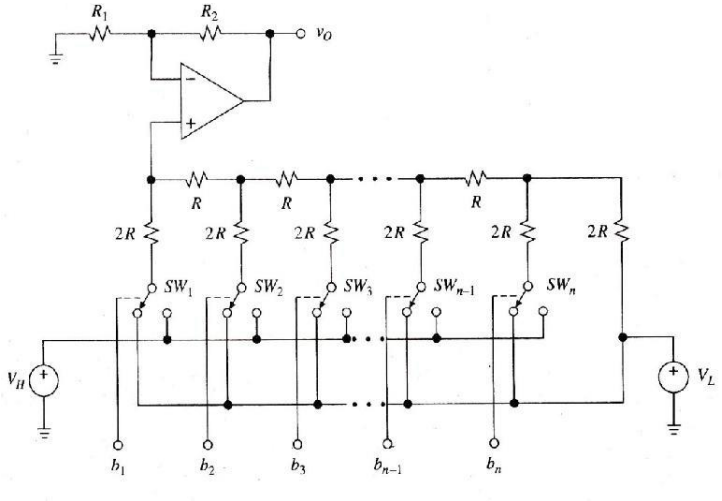


Fig. 4.6 Voltage mode DAC

The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by K = 1 + (R2/R1) results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.
2. More accurate selection and design of resistors R and 2R are possible and simple construction.
3. The binary word length can be easily increased by adding the required number or R-2R sections.

4.7 Switches for DAC

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.
ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.
iii) CMOS switch for Multiplying type DACs.
iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using overdriven Emitter Followers:

The bipolar transistors have a negligible resistance when they are operated in saturation. The bipolar transistor operating in saturation region indicates a minimum resistance and thus represents ON condition. When they are operating in cut-off region indicates a maximum resistance and thus represents OFF condition.

The circuit shown here is the arrangement of two transistors connected as emitter followers. A silicon transistor operating in saturation will have an offset voltage of 0.2V dropped across them. To have a zero offset voltage condition, the transistors must be overdriven because the saturation factor becomes negative. The two transistors Q1 (NPN) and Q2 (PNP) acts as a double pole switch. The bases of the transistors are driven by +5.75V and -5.75V.

Case 1:

When VB1 = VB2 = +5.75V, Q1 is in saturation and Q2 is OFF. And VE ≈ 5V

With VBE1 = VBE2 = 0.75V

Case 2:

When VB1 = VB2 = -5.75V, Q2 is in saturation and Q1 is OFF. And VE ≈ - 5V

With VBE1 = VBE2 = 0.75V

Thus the terminal B of the resistor Re is connected to either -5V or +5V depending on the input bit.

Switches using MOS transistor:

i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R- 2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp. The complementary outputs Q and $\overline{Q}$ drive the gates of the MOSFET M1 and M2 respectively. The SR flip flop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes Q=1 and $\overline{Q}$ =0. This makes the transistor M1 ON, thereby connecting the resistor R to reference voltage -VR. The transistor M2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes Q=0 and $\overline{Q}$ =1. This makes the transistor M2ON, thereby connecting the resistor R to Ground. The transistor M1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an opampacting as a buffer. The buffer drives the resistor R with very low output impedance.Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained intwo cases.

Case1:

When the complement of the bit line $\overline{Q}$ is low, M1 becomes ON connecting VR to thenon-inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line $\overline{Q}$ is high, M2 becomes ON connecting Ground to thenon-inverting input of the op-amp. This pulls the resistor R LOW (to ground).

CMOS switch for Multiplying type DACs:

The circuit diagram of CMOS Switch is shown here. The heart of the switching element is formedby transistors M1 and M2. The remaining transistors accept TTL or CMOS compatible logicinputs and provides the anti-phase gate drives for the transistors M1 and M2. The operation forthe two cases is as follows.

Case 1:

When the logic input is 1, M1 is ON and M2 is OFF. Thus current IK is diverted to Io bus.

Case 2:

When the logic input is 0, M2 is ON and M1 is OFF. Thus current IK is diverted to Io bus.

CMOS Transmission gate switches:

The disadvantage of using individual NMOS and PMOS transistors are threshold voltage drop (NMOS transistor passing only minimum voltage of VR- VTH and PMOS transistor passing minimum voltage of VTH). This is eliminated by using transmission gates which uses a parallel connection of both NMOS and PMOS. The arrangement shown here can pass voltages from VR to 0V acting as an ideal switch. The following cases explain the operation.

Case 1:

When the bit-line bk is HIGH, both transistors Mn and Mp are ON, offering low resistance over the entire range of bit voltages.

Case 2:

When the bit-line bk is LOW, both the transistors are OFF, and the signal transmission is inhibited (Withdrawn). Thus the NMOS offers low resistance in the lower portion of the signal and PMOS offers low resistance in the upper portion of the signal. As a combination, they offer a low parallel resistance throughout the operating range of voltage. Wide varieties of these kinds of switches were available. Example: CD4066 and CD4051.

4.8 High Speed Sample and Hold Circuits

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits [1]. The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.

As depicted by Figure 4. , in the simplest sense, an S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is verystraight forward.

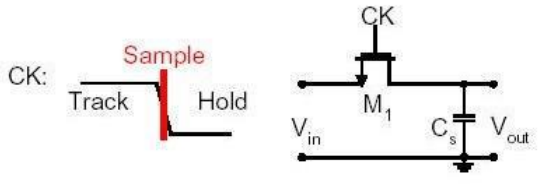


Figure 4.7 Simplest sample-and-hold circuits in MOS technology.

Figure 4, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck*is

high, the MOS switch is on, which in turn allows *Vout*to track *Vin*. On the other hand, when *ck*is low, the MOS switch is off. During this time, *Ch*will keep *Vout*equal to the value of *Vin*at the instance when *ck*goes low.

Unfortunately, in reality, the performance of this S/H circuit is not as ideal as described above. The two major types of errors occur. They are charge injection and clock feed through, that are associated with this S/H implementation. Three new S/H techniques, all of which try to minimize the errors caused by charge injection and/or clock feed through.

Alternative CMOS Sample-and-Hold Circuits

Three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feed through are

Series Sampling:

The S/H circuit of Figure 4 is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 2 is referred to as series sampling because the hold capacitor is in series with the signal.

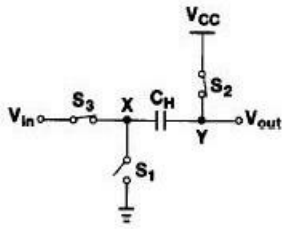


Figure 4.8 Series sampling.

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off. Then, *S2*is turned off first, which means *Vout*is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch*will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout*is now equal to *VCC –Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common- mode levels of the input and the output.

This is one advantage of series sampling over parallel sampling. In addition, unlikeparallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behaviour because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

Limitations:

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node*Y*. This parasitic capacitance introduces distortion to the sample-and hold value, thusmandating that *Ch*be much larger than the parasitic capacitance. On top of this disadvantage,the settling time of the S/H circuit during hold mode is longer for series sampling than for parallelsampling. The reason for this is because the value of *Vout*in series sampling is being reset to *VCC*

(or *VDD*) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturationregion, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor isconnected to the drain of the MOS transistor, charge injection will only go to the source junction,leaving the drain unaffected. Based on this concept, a switched op- amp (SOP) based S/H circuit, asshown in Figure 4.9

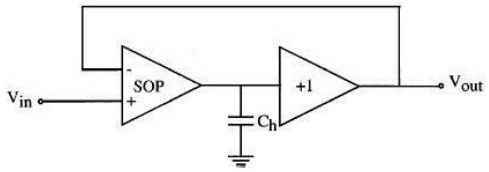


Fig. 4.9 Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP. In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on *Ch*to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on *Ch*to the output of the S/H circuit.

S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.

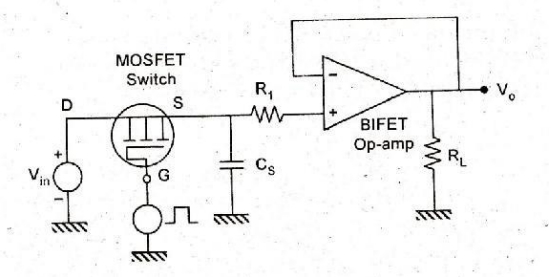


Fig.4.10 High speed Sample and Hold circuit with MOSFET

The above figure shows a sample and holds circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Three S/H circuits to reduce error:

- series sampling,
- SOP based S/H circuit,
- bottom plate S/H circuit with bootstrapped switch

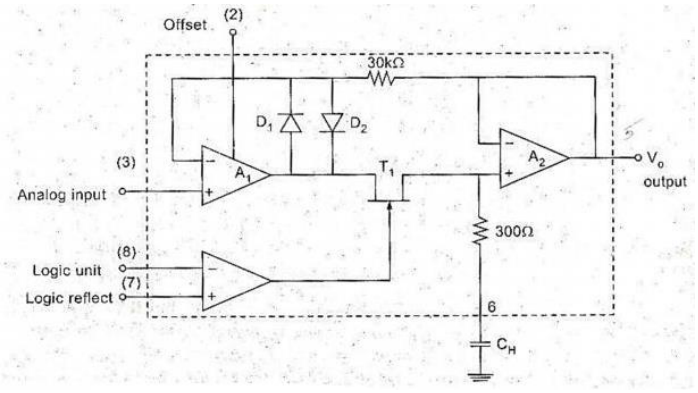


Fig.4.11 LF 398 IC- Functional Diagram

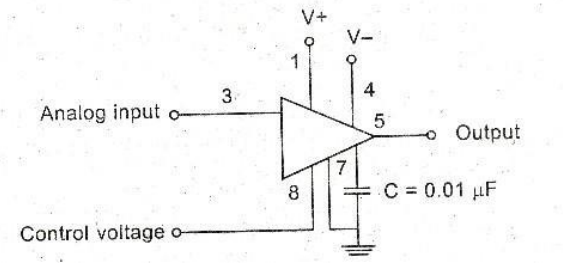


Fig.4.12 Connections of S&H IC

4.9 A to D Converter- Specifications

Like DAC, ADCs are also having many important specifications. Some of them are Resolution, Quantization error, Conversion time, Analog error, Linearity error, DNL error, INL error & Input voltage range.

Resolution:

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as $1/2^n$, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage.

Resolution can also be defined as the ratio of change in the value of input voltage Vi, needed to change the digital output by 1 LSB. It is given as

Resolution = ViFS / $(2^n - 1)$

Where 'ViFS' is the full-scale input voltage.

'n' is the number of output bits.

Quantization error:

If the binary output bit combination is such that for all the values of input voltage Vi between any two voltage levels, there is an unavoidable uncertainty about the exact value of Vi when the output is a particular binary combination. This uncertainty is termed as quantization error. Its value is ± (1/2) LSB. And it is given as,

QE = ViFS / $2(2^n - 1)$

Where 'ViFS' is the full-scale input voltage

'n' is the number of output bits.

Maximum the number of bits selected, finer the resolution and smaller the quantization error.

Conversion Time:

It is defined as the total time required for an A/D converter to convert an analog signal to digital output. It depends on the conversion technique and propagation delay of the circuit components.

Analog error:

An error occurring due to the variations in DC switching point of the comparator, resistors, reference voltage source, ripples and noises introduced by the circuit components is termed as Analog error.

Linearity Error:

It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

Differential Non-Linearity (DNL) Error:

The analog input levels that trigger any two successive output codes should differ by 1 LSB. Anydeviation from this 1 LSB value is called as DNL error.

Integral Non-Linearity (INL) Error:

The deviation of characteristics of an ADC due to missing codes causes INL error. Themaximum deviation of the code from its ideal value after nulling the offset and gain errorsis called as Integral Non-Linearity Error.

Input Voltage Range:

It is the range of voltage that an A/D converter can accept as its input without causing anyoverflow in its digital output.

Analog Switches

There were two types of analog switches. Series and Shunt switch. The Switch operation is shownfor both the cases VGS=0 VGS= VGs (off)

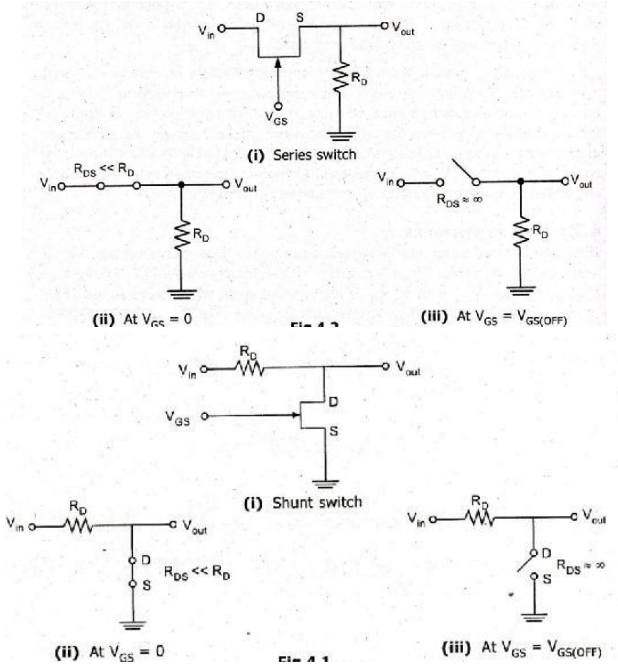


Fig 4.13 Series and shunt Analog switches

4.10 Direct-conversion ADC/Flash type ADC:

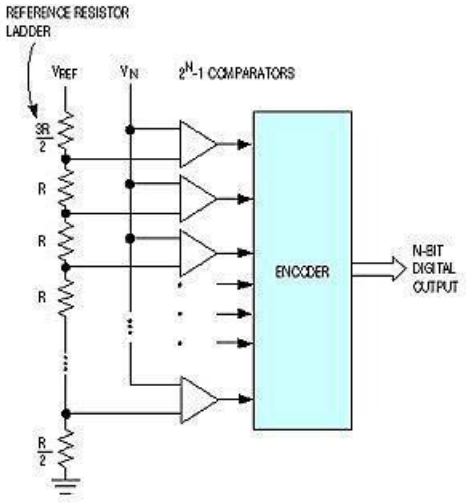


Fig.4.14 Flash ADC

This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.

4.12 Successive-approximation ADCs

Successive-approximation ADC is a conversion technique based on a successive approximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC).

The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost. A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved.

At each step in this process, a binary value of the approximation is stored in asuccessive approximation register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons.

For example if the input voltage is 60 V and the reference voltage is 100 V, in the 1st clock cycle, 60 V is compared to 50 V (the reference, divided by two. This is the voltage at the output of the internal DAC when the input is a '1' followed by zeros), and the voltage from the comparator is positive (or '1') (because 60 V is greater than 50 V). At this point the first binary digit (MSB) is set to a '1'. In the 2nd clock cycle the input voltage is compared to 75 V (being halfway between 100 and 50 V: This is the output of the internal DAC when its input is '11' followed by zeros) because 60 V is less than 75 V, the comparator output is now negative (or '0'). The second binary digit is therefore set to a '0'. In the 3rd clock cycle, the input voltage is compared with 62.5 V (halfway between 50 V and 75 V: This is the output of the internal DAC when its input is '101' followed by zeros). The output of the comparator is negative or '0' (because 60 V is less than 62.5 V) so the third binary digit is set to a 0. The fourth clock cycle similarly results in the fourth digit being a '1' (60 V is greater than 56.25 V, the DAC output for

'1001' followed by zeros). The result of this would be in the binary form 1001. This is also called *bit-weighting conversion*, and is similar to a binary.

The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired.

The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required.

ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

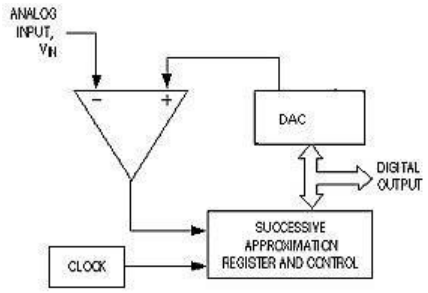


Fig.4.15 Successive approximation ADC

4.13 Dual slope ADC (Integrating ADCs)

In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again.

The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period.

The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution.

Use: Converters of this type (or variations on the concept) are used in most digital Voltmeters for their linearity and flexibility.

4.14 A/D Using Voltage to Time Conversion:

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram a negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va.

At t = T, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.

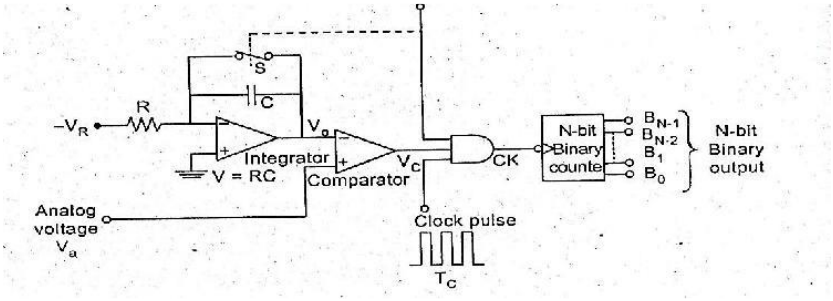


Fig. 4.16 A/D Using Voltage to Time Conversion:

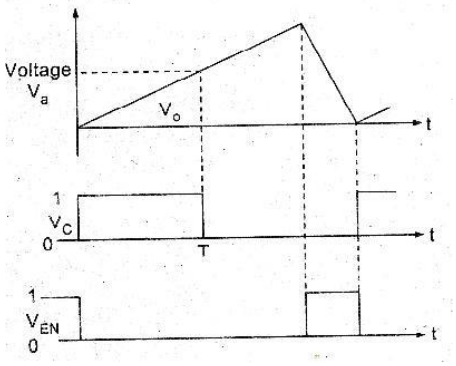


Fig.4.17 Conversion process

4.15 Sigma-delta ADCs/ Over sampling Converters:

It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal, converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, Low noise and low cost. Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.

A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (Sigma-delta modulation, also called delta-sigma modulation).

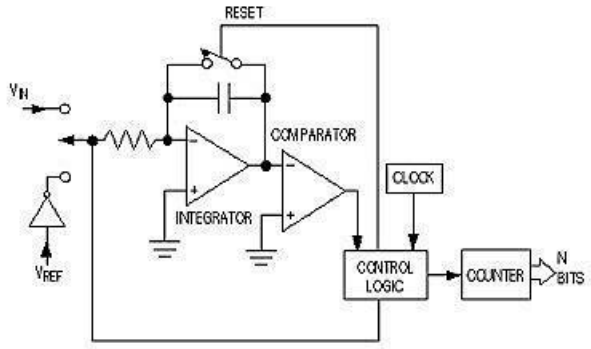
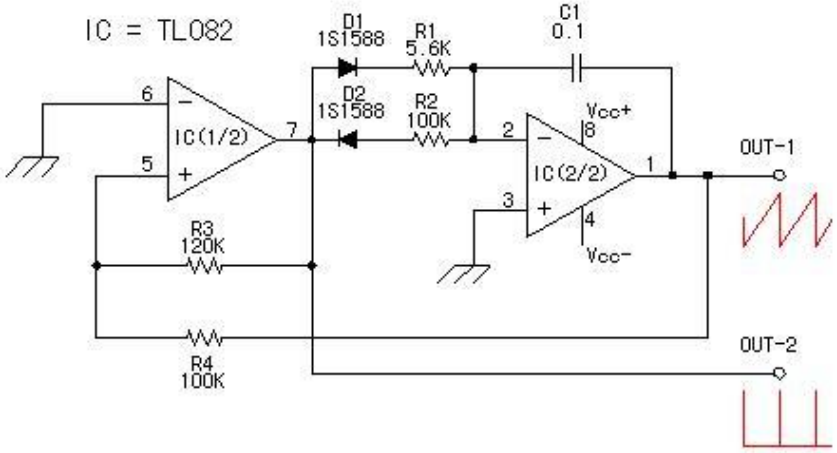


Fig 4.18 Sigma-delta ADCs/ Over sampling Converters:

UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICS

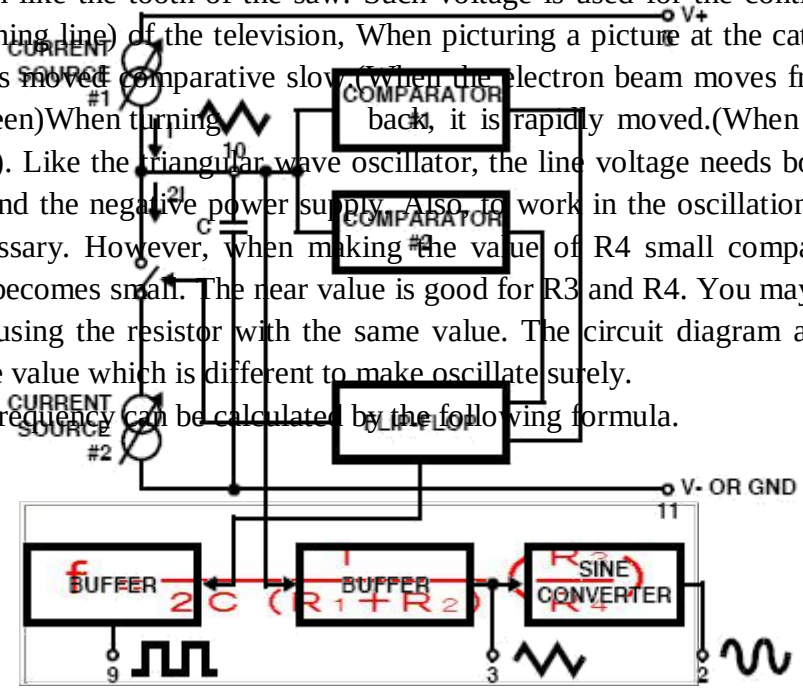
SAW-TOOTH WAVE GENERATOR

Circuit Diagram:



The sawtooth wave oscillator which used the operational amplifier. The composition of this circuit is the same as the triangular wave oscillator basically and is using two operational amplifiers. At the circuit diagram above, IC(1/2) is the Schmitt circuit and IC(2/2) is the Integration circuit. The difference with the triangular wave oscillator is to be changing the time of the charging and the discharging of the capacitor. When the output of IC(1/2) is positive voltage, it charges rapidly by the small resistance(R1) value.(When the integration output voltage falls) When the output of IC(1/2) is negative voltage, it is made to charge gradually at the big resistance(R2) value. The output waveform of the integration circuit becomes a form like the tooth of the saw. Such voltage is used for the control of the electron beam (the scanning line) of the television, When picturing a picture at the cathode-ray tube, an electron beam is moved comparative slow (When the electron beam moves from the left to the right on the screen)When turning back, it is rapidly moved.(When moving from the right to the left). Like the triangular wave oscillator, the line voltage needs both of the positive power supply and the negative power supply. Also, to work in the oscillation, the condition of R3>R4 is necessary. However, when making the value of R4 small compared with R3, the output voltage becomes small. The rear value is good for R3 and R4. You may make opposite if not oscillating using the resistor with the same value. The circuit diagram above is using the resistor with the value which is different to make oscillate surely.

The oscillation frequency can be calculated by the following formula.



FUNCTION GENERATOR IC 8038

It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter.

Pin description:

Pin 1 & Pin 12: Sine wave adjusts:

The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

Pin 2 Sine Wave Output:

Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc.

Where ± 5V ≤ Vcc ≤ ± 15 V.

Pin 3 Triangular Wave output:

Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

Pin 4 & Pin 5 Duty cycle / Frequency adjust:

The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

Pin 6+ Vcc:

Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

Pin 7 : FM Bias:

This pin along with pin no8 is used to TEST the IC 8038.

Pin9 : Square Wave Output:

A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very useful in making the square wave output.

Pin 10 : Timing Capacitors:

The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

Pin 11 : $-V_{EE}$ or Ground:

If a single polarity supply is to be used then this pin is connected to supply ground & if (±) supply voltages are to be used then (-) supply is connected to this pin.

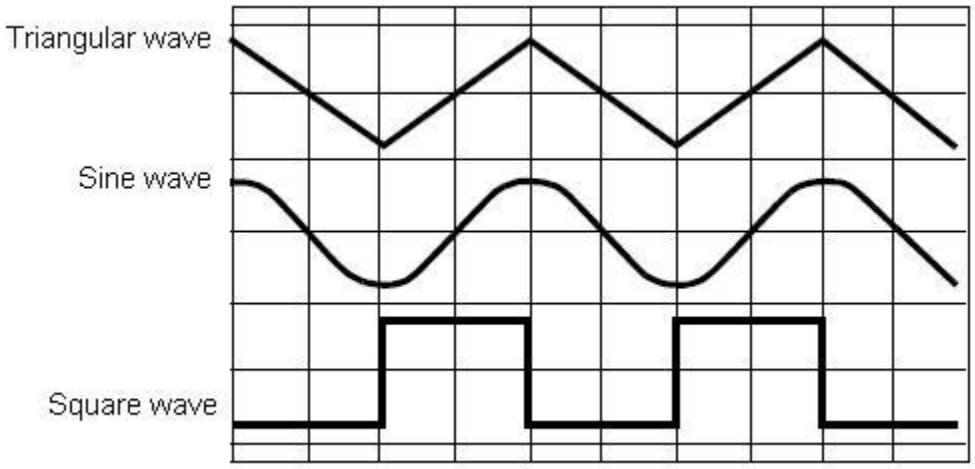
Pin 13 & Pin 14: NC(No Connection)

Important features of IC 8038:

All the outputs are simultaneously available.

1. Frequency range : 0.001Hz to 500kHz
2. Low distortion in the output wave forms.
3. Low frequency drift due to change in temperature.
4. Easy to use.

Output Waveform:



THE 555 TIMER IC

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

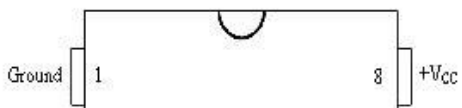
The important features of the 555 timer are these:

(i) It operates on +5v to +18 v supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p



PIN CONFIGURATION OF 555 TIMER:

Pin description:

Pin 1: Ground:

All voltages are measured with respect to this terminal.

Pin 2: Trigger:

The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3: Output:

There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage

(Between Pin 3 & Ground ON load)

(Between Pin 3 & + Vcc OFF load)

(i) When the input is low:

The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(ii) When the output is high:

The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

Pin 4: Reset:

The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage:

An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold:

This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge:

This pin is connected internally to the collector of transistor Q1.

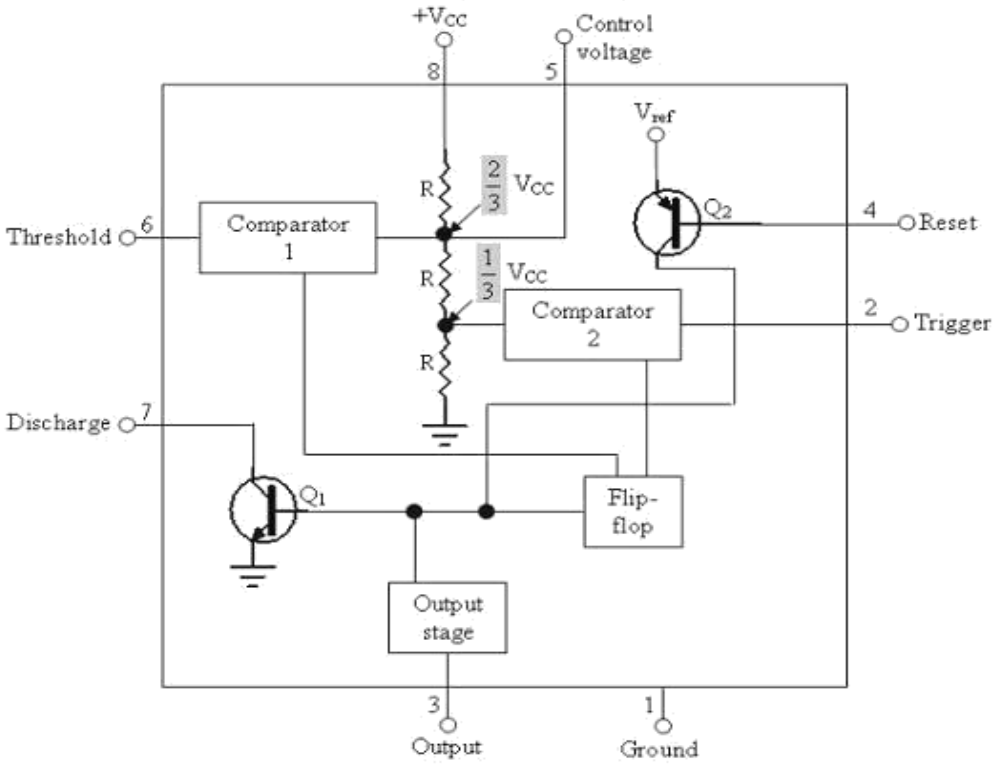
When the output is high Q1 is OFF.

When the output is low Q is (saturated) ON.

Pin 8: +Vcc:

The supply voltage of +5V to +18V is applied to this pin with respect to ground.

Block Diagram of 555 Timer IC:



From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

(i) In the Stable state:

The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

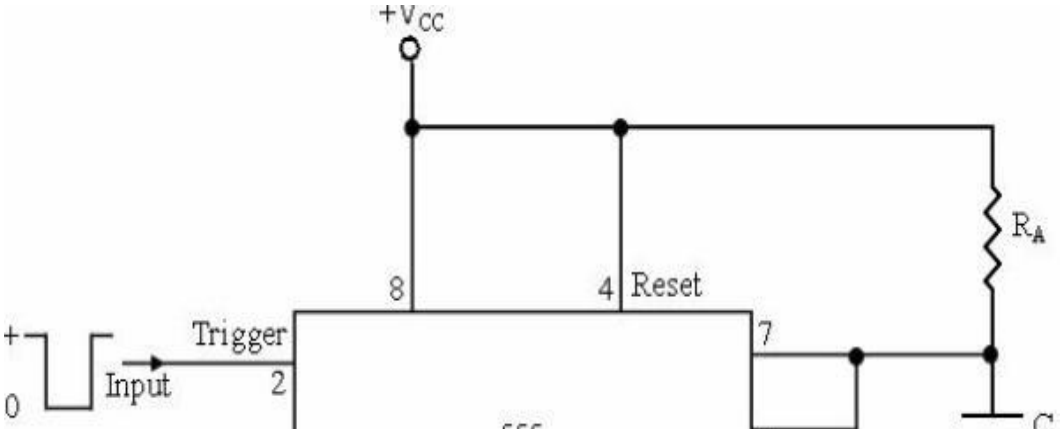
(ii) At the Negative going trigger pulse:
The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0

(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator

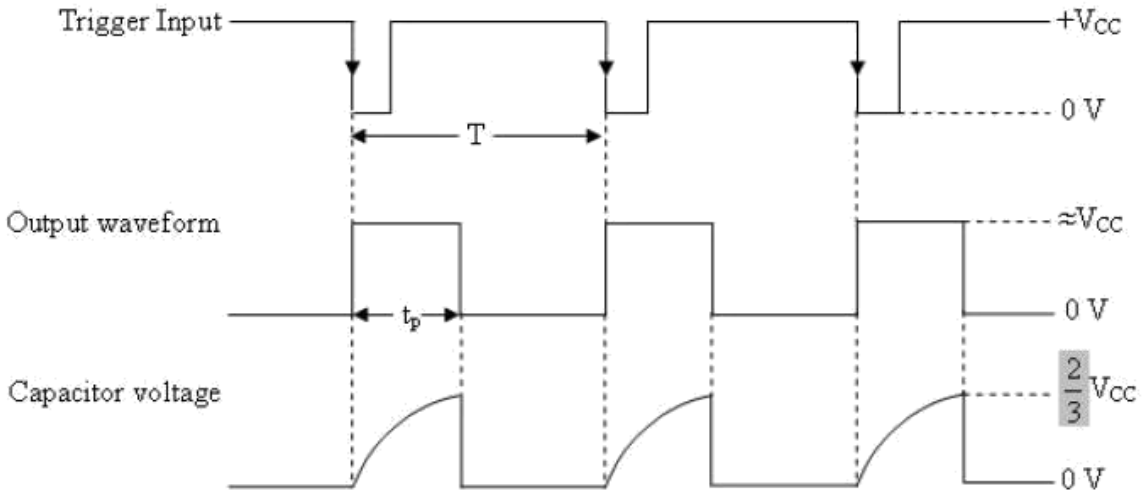
goes high and resets the FF. Q = 0; Q = 1

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

Monostable Operation:

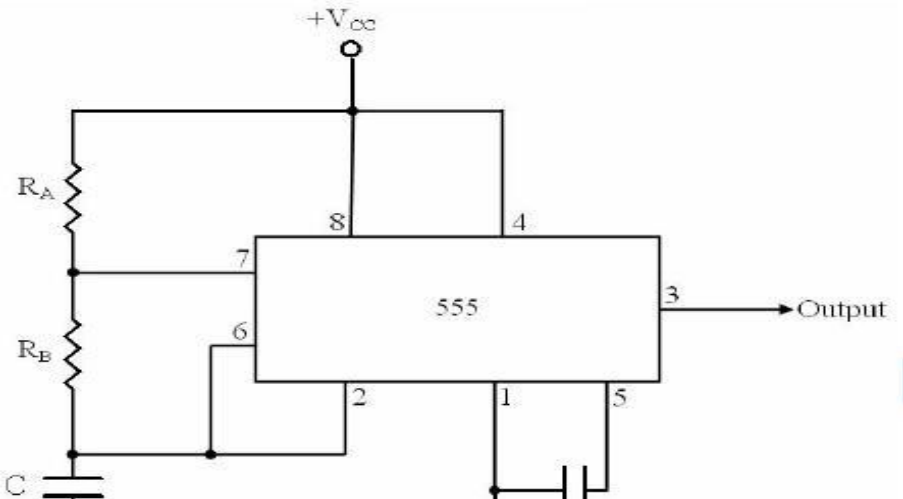


Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through R_A. When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high.



The 555 timer as an AstableMultivibrator:

An Astablemultivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostablemultivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.



Initially, when the output is high :

Capacitor C starts charging toward Vcc through R_A& R_B. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through R_B and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes High. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc& 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

$t_c = (R_A+R_B)C \ln 2$ ……(1) Where [ln 2 = 0.69]

$= 0.69 (R_A+R_B)C$

Where R_A&R_B are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

$t_c = R_B C \ln 2$

$t_d = 0.69 R_B C$ ……..(2)

where R_B is in ohms and C is in farads.

Thus the total period of the output waveform is

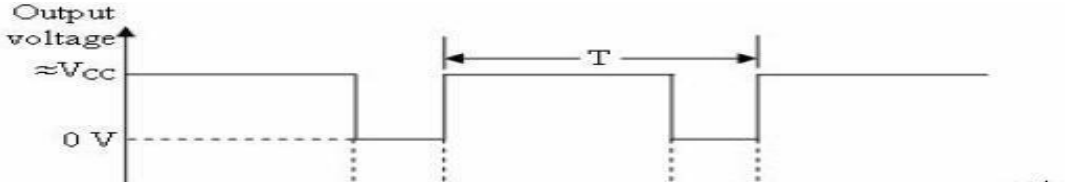
$T = t_c + t_d = 0.69 (R_A+2R_B)C$ …….(3)

This, in turn, gives the frequency of oscillation as, $f_0 = 1/T = 1.45/(R_A+2R_B)C$ ……(4)

Equation (4) indicates that the frequency f_0 is independent of the supply voltage Vcc. Often the term duty cycle is used in conjunction with the astablemultivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage.

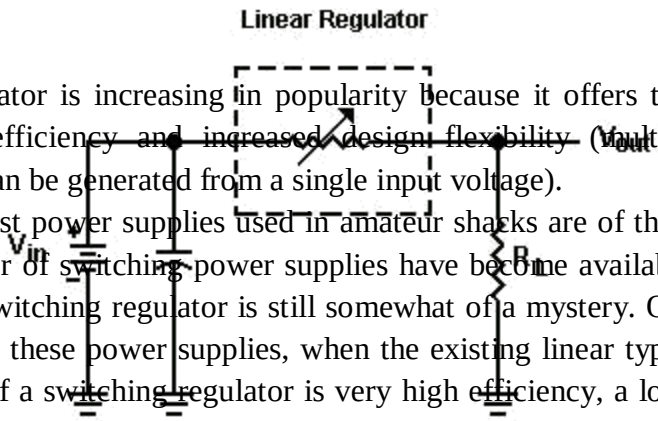
duty cycle = $(t_c / T)* 100$

DC = $[(R_A+R_B)/ /(R_A+2R_B)] * 100$



SWITCHING REGULATORS

Introduction



The switching regulator is increasing in popularity because it offers the advantages of higher power conversion efficiency and increased design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).

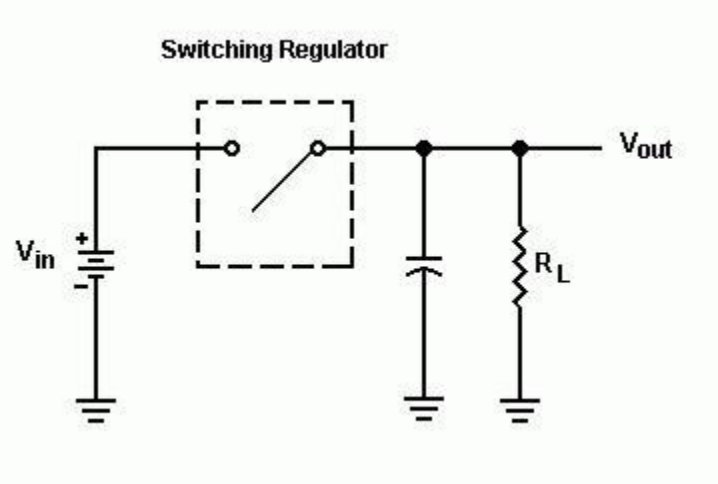
Although most power supplies used in amateur shacks are of the linear regulator type, an increasing number of switching power supplies have become available to the amateur. For most amateurs the switching regulator is still somewhat of a mystery. One might wonder why we even bother with these power supplies, when the existing linear types work just fine. The primary advantage of a switching regulator is very high efficiency, a lot less heat and smaller size. To understand how these black boxes work lets take a look at a traditional linear regulator at right. As we see in the diagram, the linear regulator is really nothing more than a variable resistor. The resistance of the regulator varies in accordance with the load resulting in a constant output voltage

The primary filter capacitor is placed on the input to the regulator to help filter out the 60 cycle ripple. The linear regulator does an excellent job but not without cost. For example, if the output voltage is 12 volts and the input voltage is 24 volts then we must drop 12 volts across the regulator.

The time that the switch remains closed during each switch cycle is varied to maintain a constant output voltage. Notice that the primary filter capacitor is on the output of the regulator and not

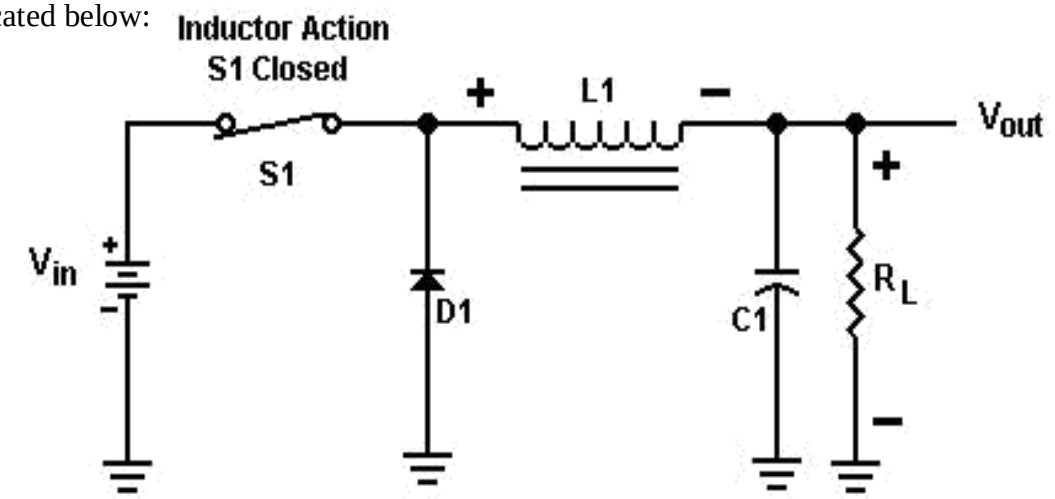
the input. As is apparent, the switching regulator is much more efficient than the linear regulator achieving efficiencies as high as 80% to 95% in some circuits. The obvious result is smaller heat sinks, less heat and smaller overall size of the power supply.

At output currents of 10 amps this translates into 120 watts (12 volts times 10 amps) of heat energy that the regulator must dissipate. Is it any wonder why we have to use those massive heat sinks? As we can see this results in a mere 50% efficiency for the linear regulator and a lot of wasted power which is normally transformed into heat.

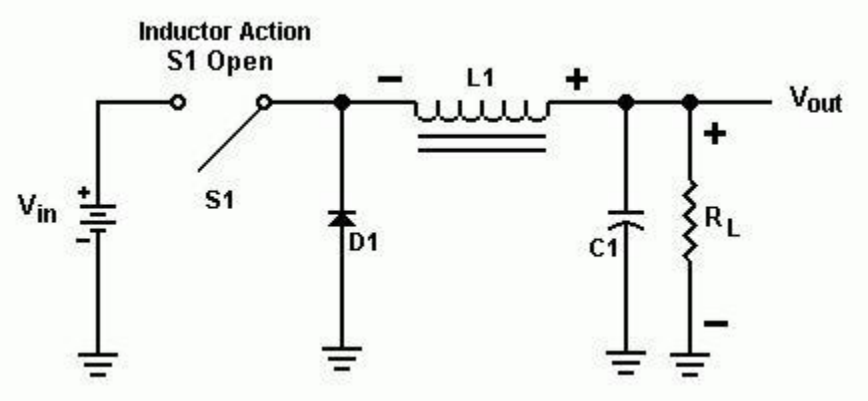


As we see above the switching regulator appears to have a few more components than a linear regulator. Diode D1 and Inductor L1 play a very specific role in this circuit and are found in almost every switching regulator. First, diode D1 has to be a Schottky or other very fast switching diode. A 1N4001 just won't switch fast enough in this circuit. Inductor L1 must be a type of core that does not saturate under high currents. Capacitor C1 is normally a low ESR (Equivalent Series Resistance) type.

To understand the action of D1 and L1, lets look at what happens when S1 is closed as indicated below:



As we see above, L1, which tends to oppose the rising current, begins to generate an electromagnetic field in its core. Notice that diode D1 is reversed biased and is essentially an open circuit at this point. Now lets take a look at what happens when S1 opens below:



As we see in this diagram the electromagnetic field that was built up in L1 is now discharging and generating a current in the reverse polarity. As a result, D1 is now conducting and will continue until the field in L1 is diminished. This action is similar to the charging and discharging of capacitor C1. The use of this inductor/diode combination gives us even more efficiency and augments thefilteringof C1. Because of the unique nature of switching regulators, very special design considerations are required. Because the switching system operates in the 50 to 100 kHz region and has an almost square waveform, it is rich in harmonics way up into the HF and even the VHF/UHF region. Special filtering is required, along with shielding, minimized lead lengths and all sorts of toroidal filters on leads going outside the case. The switching regulator also has a minimum load requirement, which is

determined by the inductor value. Without the minimum load, the regulator will generate excessive noise and harmonics and could even damage itself. (This is why it is not a good idea to turn on a computer switching power supply without some type of load connected.) To meet this requirement, many designers use a cooling fan and or a minimum load which switches out whenno longer needed.

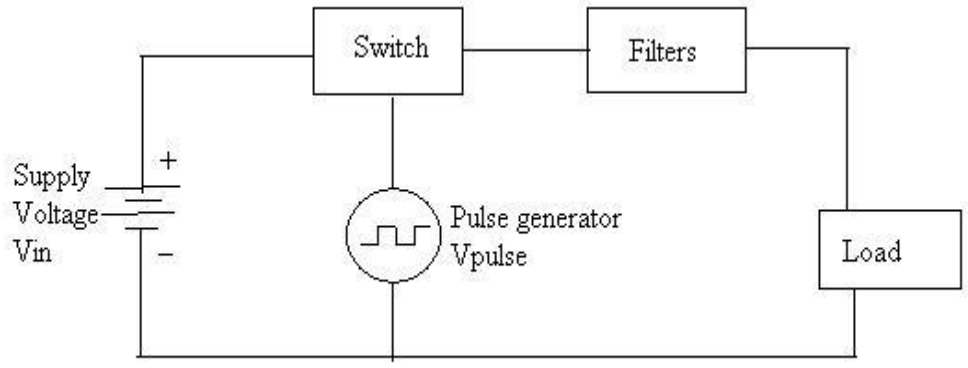
SWITCHING REGULATOR:

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

To minimize the power dissipation during switching, the external transistor used must be a switching power transistor.

To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

- A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
- This output is filtered through a low pass LC filter to produce an average dc output voltage.
- Thus the output voltage is proportional to the pulse width and frequency.
- The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%



A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.

- It must be large enough to supply sufficient dynamic range for line & load regulations.
- It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.
- It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF.

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage. Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.

THE SWITCHED CAPACITOR FILTER

The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S_1 and S_2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge *q* from the input to the output at the switching frequency *f*. Recall that the charge *q* on a capacitor *C* with a voltage *V* between the plates is given by:

$$q = CV$$

where$V$ is the voltage across the capacitor. Therefore, when S_1 is closed while S_2 is open, the charge transferred from the source to C_S is:

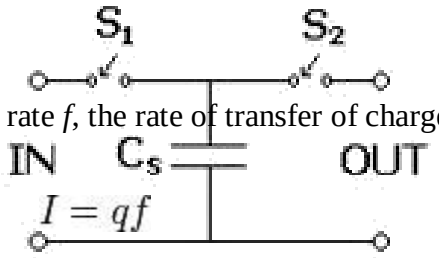
$$q_{IN} = C_S V_{IN}$$

and when S_2 is closed while S_1 is open, the charge transferred from C_S to the load is:

$$q_{OUT} = C_S V_{OUT}$$

Thus, the charge transferred in each cycle is:

$$q = q_{OUT} - q_{IN} = C_S(V_{OUT} - V_{IN})$$



Since a charge q is transferred at a rate f, the rate of transfer of charge per unit time is:

3.

Note that we use I, the symbol for electric current, for this quantity. This is to demonstrate that a continuous transfer of charge from one node to another is equivalent to a current. Substituting for q in the above, we have:

$$I = C_S(V_{OUT} - V_{IN})f$$

Let us define V, the voltage across the SC from input to output, thus:

$$V = V_{OUT} - V_{IN}$$

We now have a relationship between I and V, which we can rearrange to give an equivalent resistance *R*:

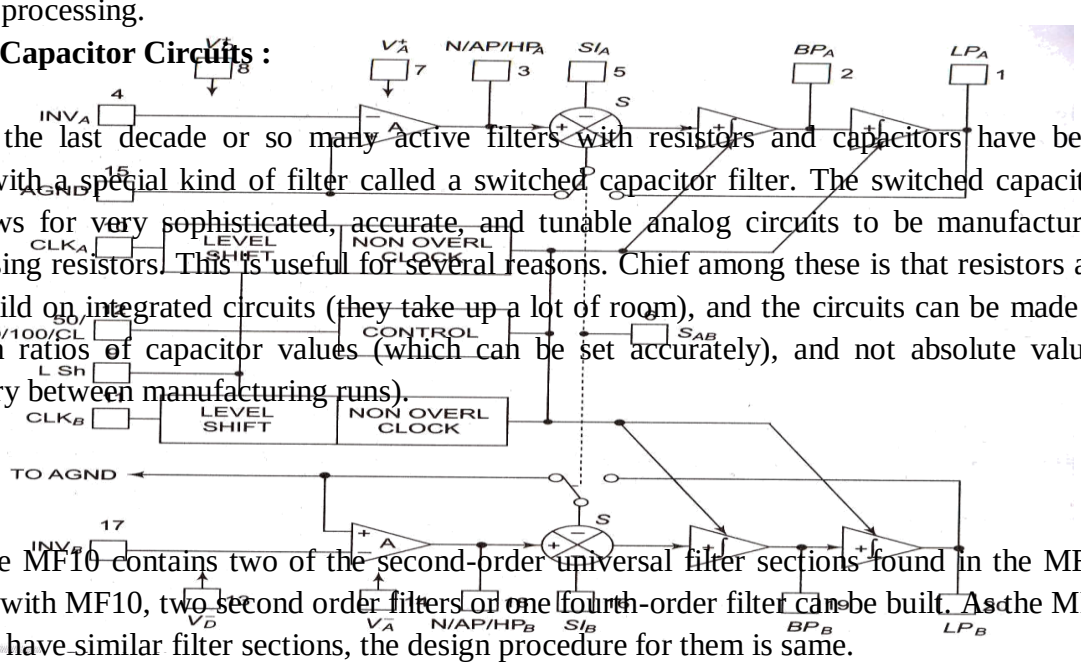
$$R = \frac{V}{I} = \frac{1}{C_S f}$$

Thus, the SC behaves like a resistor whose value depends on C_S and *f*.

The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency. See also: operational amplifier applications. This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

Switched Capacitor Circuits :

In the last decade or so many active filters with resistors and capacitors have been replaced with a special kind of filter called a switched capacitor filter. The switched capacitor filter allows for very sophisticated, accurate, and tunable analog circuits to be manufactured without using resistors. This is useful for several reasons. Chief among these is that resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).



MF10:

The MF10 contains two of the second-order universal filter sections found in the MF5. Therefore with MF10, two second order filters or one fourth-order filter can be built. As the MF5 and MF10 have similar filter sections, the design procedure for them is same.

OPTOCOUPLERS/OPTOISOLATORS:

- Optocouplers or Optoisolators is a combination of light source & light detector in the same package.
- They are used to couple signal from one point to other optically, by providing a completer electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.
- Depending on the type of light source & detector used we can get a variety of optocouplers. They are as follows,
  - (i) LED – LDR optocoupler
  - (ii) LED – Photodiode optocoupler
  - (iii) LED – Phototransistor optocoupler

Characteristics of optocoupler:

(i) Current Transfer Ratio (CTR)

(ii) Isolation Voltage

(iii) Response Time

(iv) Common Mode Rejection

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the inputforward current (If)

CTR = Ic/If * 100%

Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between theinput& output without affecting the electrical isolation voltage isspecified in K Vrms with a relative humidity of 40 to 60%.

(iii)Response Time:

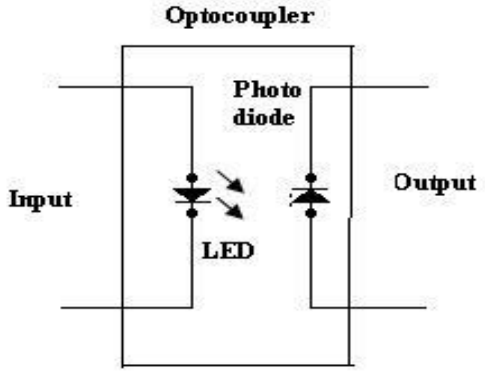
Response time indicates how fast an optocoupler can change its outputstate. Response time largely depends on the detector transistor, inputcurrent & load resistance.

(iv)Common mode Rejection:

Eventhough the optocouplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allow the noise to appear in the output.

Types of optocoupler:

(i) LED – Photodiode optocoupler:



LED photodiode shown in figure, here the infrared LED acts as a light source & photodiode is used as a detector.

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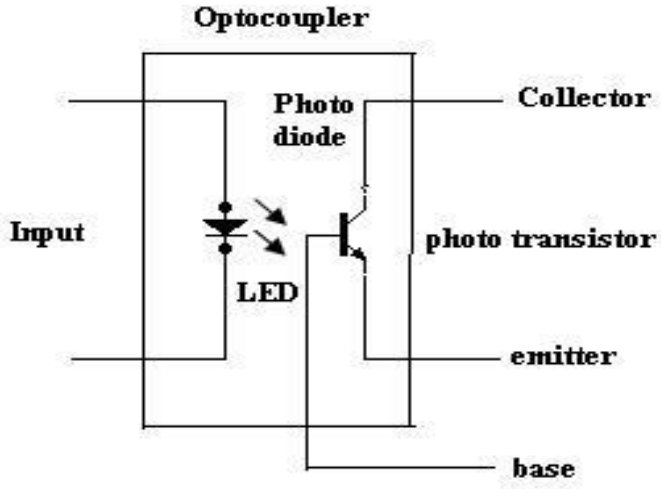
The advantage of using the photodiode is its high linearity. When the pulse at the input goes high, the LED turns ON. It emits light. This light is focused on the photodiode.

In response to this light the photocurrent will start flowing though the photodiode. As soon as the input pulse reduces to zero, the LED turns OFF & the photocurrent through the photodiode reduces to zero. Thus the pulse at the input is coupled to the output side.

(ii) LED – Phototransistor Optocoupler:



The LED phototransistor optocoupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.

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- This is the most popularly used optocoupler, because it does not need any additional amplification. When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.
  In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.
- The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.

Advantages of Optocoupler:

- Control circuits are well protected due to electrical isolation.
- Wideband signal transmission is possible.
- Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.
- Interfacing with logic circuits is easily possible.It is small size & light weight device.

Disadvantages:

- Slow speed.
- Possibility of signal coupling for high power signals.

Applications:

- Optocouplers are used basically to isolate low power circuits from highpower circuits.
  At the same time the control signals are coupled from the control circuits to the high power
- circuits. Some of such applications are,

(i) AC to DC converters used for DC motor speed control

(ii) High power choppers

(iii) High power inverters

- One of the most important applications of an optocoupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.
- Note that the input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor.

Optocoupler IC:

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.

- This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.
- The infrared radiation from the LED gets focused on the internal phototransistor.
- The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.
- The block diagram shows the opto-electronic integrated ciruit (OEIC) and the major components of a fiber-optic communication facility.